Algorithm 9xx: Sparse QR Factorization on the GPU

SENCER NURI YERALAN, University of Florida
TIMOTHY A. DAVIS, Texas A&M University
WISSAM M. SID-LAKHDAR, Texas A&M University
SANJAY RANKA, University of Florida

Sparse matrix factorization involves a mix of regular and irregular computation, which is a particular challenge when trying to obtain high-performance on the highly parallel general-purpose computing cores available on graphics processing units (GPUs). We present a sparse multifrontal QR factorization method that meets this challenge, and is significantly faster than a highly optimized method on a multicore CPU. Our method factorizes many frontal matrices in parallel and keeps all the data transmitted between frontal matrices on the GPU. A novel bucket scheduler algorithm extends the communication-avoiding QR factorization for dense matrices, by exploiting more parallelism and by exploiting the staircase form present in the frontal matrices of a sparse multifrontal method.

Categories and Subject Descriptors: G.1.3 [Numerical Analysis]: Numerical Linear Algebra—linear systems (direct methods), sparse and very large systems; G.4 [Mathematics of Computing]: Mathematical Software—algorithm analysis, efficiency

General Terms: Algorithms, Experimentation, Performance

Additional Key Words and Phrases: QR factorization, least-square problems, sparse matrices, GPU

ACM Reference Format:
DOI: http://dx.doi.org/10.1145/0000000.0000000

1. INTRODUCTION

QR factorization is an essential kernel in many problems in computational science. It can be used to find solutions to sparse linear systems, sparse linear least squares problems, eigenvalue problems, rank and null-space determination, and many other mathematical problems in numerical linear algebra [Golub and Van Loan 2012]. Although QR factorization and other sparse direct methods form the backbone of many applications in computational science, the methods are not keeping pace with advances in heterogeneous computing architectures, in which systems are built with multiple general-purpose cores in the CPU, coupled with one or more General Purpose Graphics Processing Units (GPGPUs) each with hundreds or thousands of simple yet fast computational cores. The challenge for computational science is for these algorithms to adapt to this changing landscape.

Portions of this work were supported by the National Science Foundation, under grant DMS-1115297.

ACM Transactions on Mathematical Software, Vol. 1, No. 1, Article 1, Publication date: May 2016.
The computational workflow of sparse QR factorization [Amestoy et al. 1996; Davis 2011; Buttari 2013] is structured as a tree, where each node is the factorization of a dense submatrix (a frontal matrix [Duff and Reid 1983]). The edges represent an irregular data movement in which the results from a child node are assembled into the frontal matrix of the parent. Each child node can be computed independently. An assembly phase after the children are executed precedes the factorization of their parent. In this paper, we present a GPU-efficient algorithm for multifrontal sparse QR factorization that uses this tree structure and relies on a novel multifrontal algorithm for QR factorization that exploits the architectural features of a GPU. It leverages dense QR factorization at multiple levels of the tree to achieve high performance.

The main contributions of our paper are:

— A novel sparse QR factorization method that exploits the GPU by factorizing multiple frontal matrices at the same time, while keeping all the data on the GPU. The result of one frontal matrix (a contribution block) is assembled into the parent frontal matrix on the GPU, with no data transfer to/from the CPU.

— A novel scheduler algorithm that extends the Communication-Avoiding QR factorization [Demmel et al. 2012]. We extend this method to factorize multiple panels of the matrix simultaneously, thereby increasing parallelism and reducing the number of kernel launches in the GPU. The algorithm is flexible in the number of threads/SMs used for concurrently executing multiple dense QRs (of potentially different sizes). At or near the leaves of the tree, each SM works on its own frontal matrix. Further up the tree, multiple SMs collaborate to factorize a frontal matrix.

— The scheduling algorithm and software does not assume that the entire problem will fit in the memory of a single GPU. Rather, we move subtrees into the GPU, factorize them, and then move the resulting contribution block (of the root of the subtree) and the resulting factor (just $R$, since we discard $Q$) out of the GPU. This data movement between the CPU RAM and the GPU RAM is expensive, since it moves across the relatively slow PCI bus. We double-buffer this data movement, so that we can be moving data to/from the GPU for one subtree, while the GPU is working on another.

— For large sparse matrices, the GPU-accelerated algorithm offers up to 11x speedup over CPU-based QR factorization methods, with a median speedup of 5x for large matrices. It achieves up to 200 GFlops as compared to a peak of 79 GFlops for the same algorithm on a multicore CPU.

Section 2 presents the background of sparse QR factorization and the GPU computing model. The main components of the parallel QR factorization algorithm are given in Section 3. In Section 4, we compare the performance of our GPU-accelerated sparse QR to Davis’ SuiteSparseQR package on a large set of matrices from real applications [Davis and Hu 2011]. SuiteSparseQR is the sparse QR factorization in MATLAB [Davis 2011]. It uses LAPACK [Anderson et al. 1999] for panel factorization and block Householder updates, whereas our GPU-accelerated code uses our GPU compute kernels for this update step. Future work in this algorithm is discussed in Section 5. An overview of related work, and a summary of this work, are presented in Sections 6 and Sections 7. Our code is available as Collected Algorithm 9xx of the ACM, and at SuiteSparse.com.

2. PRELIMINARIES

An efficient sparse QR factorization is an essential kernel in many problems in computational science. Application areas that can exploit our GPU-enabled parallel sparse QR factorization are manifold. In our widely used and actively growing SuiteSparse Matrix Collection (formerly known as the University of Florida Sparse Matrix Collection) [Davis and Hu 2011], we have problems from structural engineering, computa-
tional fluid dynamics, model reduction, electromagnetics, semiconductor devices, thermodynamics, materials, acoustics, computer graphics/vision, robotics/kinematics, optimization, circuit simulation, economic and financial modeling, theoretical and quantum chemistry, chemical process simulation, mathematics and statistics, power networks, social networks, text/document networks, web-hyperlink networks, and many other discretizations, networks, and graphs. Although only some of these domains specifically require QR factorization, most require a sparse direct or iterative solver. We view our QR factorization method as the first of many sparse direct methods for the GPU, since QR factorization is representative of many other sparse direct methods with both irregular coarse-grain parallelism and regular fine-grain parallelism.

In the next section, we briefly describe the multifrontal sparse QR factorization method and explain why we have selected it as our target for a GPU-based method. We then give an overview of the GPU computing landscape, which provides a framework for understanding the challenges we addressed as we developed our algorithm.

2.1. Multifrontal Sparse QR Factorization

2.1.1. Ordering and Analysis phase. The first step in solving a sparse system of equations \( Ax = b \) or solving a least squares problem is to permute the matrix \( A \) so that the resulting factors have fewer nonzeros than the factors of the unpermuted matrix. This step is NP-hard, but many efficient heuristics are available [Davis et al. 2004a; 2004b; Davis 2006].

The second step is to analyze the matrix to set up the parallel multifrontal numerical factorization. This step finds the elimination tree, the multifrontal assembly tree, the nonzero pattern of the factors, and the sizes of each frontal matrix. In a multifrontal method, the data flows only from child to parent in the tree, which makes the tree suitable for exploiting coarse-grain parallelism, where independent subtrees are handled on widely separated processors. The analysis takes time that is no worse than (nearly) proportional to the number of integers required to represent the nonzero pattern of the factors, plus the number of nonzeros in \( A \). This can be much less than the number of nonzeros in the factors themselves.

The ordering and analysis steps are based on our existing multifrontal sparse QR method (SuiteSparseQR) [Davis 2011]. The ordering and analysis phase is very irregular in its computation and is thus best suited to stay on the CPU.

Each node in the tree represents one or more nodes in the column elimination tree. The latter tree is defined purely by the nonzero pattern of \( R \), where the parent of node \( i \) is \( j \) if \( j > i \) is the smallest row index for which \( r_{ij} \) is nonzero. There is one node in column elimination tree for each column of \( A \).

A multifrontal assembly tree is obtained by merging nodes in the column elimination tree. A parent \( j \) and child \( j - 1 \) are merged if the two corresponding rows of \( R \) have identical nonzero pattern (excluding the diagonal entry in the child). In general, this requirement is relaxed, so that a parent and child can be merged if their patterns are similar but not necessarily identical (this is called relaxed amalgamation [Ashcraft and Grimes 1989]). Figures 1 and 2 gives an example of both trees, and the related \( A \) and \( R \) matrices. In the figure, the rows of \( A \) are sorted according to the column index of the leftmost nonzero in each row, so as to clarify the next step, which is the assembly of rows of \( A \) into the frontal matrices. Each \( x \) is a nonzero in \( A \). Each dot is an entry that will become nonzero as the matrix is factorized. Each \( r \) is a nonzero in \( R \). Each node of the tree is a column of \( A \) or row of \( R \), and they are grouped together when adjacent rows of \( R \) have the same nonzero pattern.

In the assembly process, the incoming data for a frontal matrix is concatenated together to construct the frontal matrix. No flops are performed. Each row of \( A \) is assembled into a single frontal matrix. If the leftmost nonzero of row \( i \) is in column \( j \), then
row $i$ is assembled into the frontal matrix containing node $j$ of the elimination tree. Figure 3 illustrates a leaf frontal matrix with no children in the assembly tree. It is the first frontal matrix, and contains nodes 1 and 2 of the column elimination tree. Six rows of $A$ have leftmost nonzeros in columns 1 or 2. These are concatenated together to form a 6-by-5 frontal matrix, held as a 6-by-5 dense matrix. Note that the dimensions of a frontal matrix are typically much smaller than the dimensions of $A$ itself. The frontal matrix does include some explicit zero entries, in the first column. This is due to the amalgamation of the two nodes into the front.

2.1.2. Factorization phase. This is where the bulk of the floating-point operations are performed (the remainder are done in the next step, the solve phase). All of the flops are computed within small dense frontal matrices (small relative to the dimensions of $A$, to be precise; the frontal matrices can be quite large). These computations are very regular, very compute-intensive (relative to the memory traffic requirements), and thus well-suited to be executed on one or more GPUs. Continuing the example in Figure 2, after the 6 rows of $A$ are assembled into the front, we compute its QR factor-
ization, reflected in the matrix on the right side of Figure 3. Each \( r \) is a nonzero in \( R \), each \( h \) is a nonzero Householder coefficient, and each \( c \) is an entry in the contribution block.

![assembly and factorization of a leaf](image)

Figure 4 illustrates what happens in the factorization of a frontal matrix that is not a leaf in the tree. Three prior contribution blocks are concatenated and interleaved together, along with all rows of \( A \) whose leftmost nonzero falls in columns 5, 6, or 7 (the fully-assembled columns of this front). The QR factorization of this rectangular matrix is then computed.

![assembly and factorization of a front with children](image)

Computation across multiple CPU cores and multiple GPUs can be obtained by splitting the tree in a coarse-grain fashion. At the root of each subtree, a single contribution block would need to be sent, or distributed, to the CPU/GPU cores that handle the parent node of the tree. Our current method exploits only a single GPU, but to handle very large problems, it splits the trees into subtrees that fit in the global memory of the GPU.

### 2.1.3. Solve phase

Once the system is factorized, the factors typically need to be used to solve a linear system or least-squares problem. These computations require a number of flops proportional to the number of nonzeros in the factors. The ratio of flop count per memory reference is thus quite low. The cuSPARSE package from NVIDIA...
includes a sparse triangular solve, and thus we do not consider this phase in the scope of this paper.

2.2. GPU architecture

In general, a heterogeneous GPGPU system consists of one or more highly-flexible CPU cores, and very many high-throughput computational cores on one or more GPUs. While our algorithmic methods should extend to many different kinds of GPUs or other related platform (such as the Intel Xeon Phi), we have restricted our current implementation of our algorithms to the NVIDIA GPGPU framework based on the CUDA programming model.

An NVIDIA GPU consists of a set of SMs (Streaming Multiprocessors), each with a set of cores that operate in lock-step manner. The *shared memory* available on each SM can be accessed by all cores in the SM, but it is very limited (typically 32K to 64K bytes) and must be shared among multiple blocks of threads. Minimizing the memory traffic between slow GPU global memory and very fast shared memory is crucial to achieve high performance. Dense QR factorization has a very good compute-to-data-movement ratio and can achieve high performance even under these limitations.

The GPU executes one or more *kernels*, which are launched by the CPU. When launching a kernel, the programmer specifies a number of *thread blocks* and the number of threads per block the GPU should commit to the kernel launch. These kernel launch parameters describe how the work is intended to be divided by the GPU among its SMs, and GPUs have varying upper bounds on the allowed parameter values. Regardless of the number of available SMs or cores per SM for a particular GPU, the GPU’s scheduler assigns thread blocks to SMs and executes the kernel until the thread block completes its execution. The GPU scheduler organizes threads into collections of 32, called a *warp*, and threads constituting a warp execute code in a Single Program Multiple Data (SPMD) fashion within an SM [NVIDIA Corporation 2011].

Each thread on the GPU has access to a small number of registers, which cannot be shared with any other thread. New GPUs allow for some sharing of register data amongst the threads in a single warp, but our current algorithm does not exploit this feature.

Each SM has a small amount of *shared memory* that can be accessed and shared by all threads on the SM, but which is not accessible to other SMs. There is no cache coherency across multiple SMs. The shared memory is arranged in banks, and bank conflicts occur if multiple threads attempt to access different entries in the same bank at the same time. Matrices are padded to avoid bank conflicts, so that a row-major matrix of size \( m \times n \) is held in an \( m \times (n + 1) \) array when in shared memory. In this context, the \( m \times n \) matrix is a small selected subset of one of the frontal matrices being factorized by the GPU. We can thus ensure that \( n \) is a multiple of the bank size. Accessing of shared memory can be done in randomly-accessed order without penalty, so long as bank conflict is avoided.

Global memory on the GPU is large, but its bandwidth is much smaller than the bandwidth of shared memory, and the latency is higher. Global memory can be read by all SMs, but must be read with stride-one access for best performance (a *coalesced* memory transaction).

The GPU provides hardware support for fast warp-level context switching on an SM, and the GPU scheduler attempts to hide memory latency by overlapping global memory transactions with computation by switching between warps. While a memory transaction for one warp is pending, the SM executes another warp whose memory transactions are ready.

All three layers of memory (global, shared, and register) must be explicitly managed for best performance, with multiple memory transactions between each layer “in flight”
at the same time, with many warps, so that computation can proceed in one warp while another warp is waiting for its memory transaction to complete.

3. PARALLEL MULTIFRONTAL SPARSE QR FACTORIZATION ALGORITHM ON THE GPU

The computational workflow of the multifrontal QR method is structured as a tree. Each node represents the factorization of a dense submatrix. Each edge represents an irregular data movement in which the results from a child node are assembled into the frontal matrix of the parent. All child nodes can be computed independently, but an assembly phase occurs after their execution and before that of their parent. Our algorithm is flexible in the number of threads/SMs used for concurrently executing multiple dense QRs (of potentially different sizes). At or near the leaves of the tree, each SM in a GPU works on its own frontal matrix. Further up the tree, multiple SMs collaborate to factorize a frontal matrix.

The details of our algorithm are described in the following sections in a top-down perspective, starting at the high-level of the tree, and proceeding down to the low-level of work that each GPU thread performs.

1. At a high-level and from the task tree point of view, we describe in Section 3.1 how we represent the progress of the factorization of the entire tree together with the data dependencies between nodes of the tree.

2. We also describe in Section 3.2 how we break the tree into subtrees when it is too large to fit all at once on the GPU.

3. At a high-level and from the GPU point of view, we discuss in Section 3.3 the \textit{uberkernel approach}. The tree (or whatever part of it fits on the GPU) is factorized from the bottom up to the root, but each node in the tree (a single frontal matrix) is not factorized as a single task on the GPU. Rather, we break the factorization of each frontal matrix into a sequence of kernel launches. Each kernel launch operates on many fronts at a time.

4. At the mid-level of a single front, we describe in Section 3.4 the \textit{Bucket Scheduler}. The CPU creates one scheduler per frontal matrix and its job is to keep track of the current state of factorization of the corresponding front.

5. At the low-level of the GPU kernels, we describe in Section 3.5 how the GPU performs the tasks given to it by the Bucket Scheduler. This section describes how the SM performs a single task in a kernel launch, and what each thread does within that task.

3.1. Sparse QR Scheduler

The Sparse QR Scheduler manages both assembly and factorization kernel launches, coalescing the schedules of tasks from many assembly operations and many dense QR bucket schedulers into a single kernel launch. In this section, we describe the assembly operations and the tree-level parallelism. The factorization of each node in the tree is handled by the bucket scheduler described later on in Section 3.4.

Figure 5 represents an example of assembly tree. Arrows point in the direction of contribution block data flow, from child to parent. The size of each node reflects the size of the corresponding frontal matrix.

The Sparse QR Scheduler starts by activating the leaves of the assembly tree (light blue nodes in Figure 5) as these fronts have no children. When a front is activated, the scheduler builds an \textit{S-Assembly} task that will assemble the corresponding values of the input problem into the front. Then, the front must wait for contribution blocks from its children to be assembled into it (if any). Once every child of the front completes, the scheduler advances this front into factorization. A Bucket Scheduler is created for this front and is invoked to factorize it, using two types of tasks on the GPU: (1) a \textit{Factorize}
task that computes the QR factorization of a submatrix of the frontal matrix, and (2) an Apply task that applies the resulting block Householder update to the right of this submatrix. Once dense factorization of the front completes, its rows of the result, the $R$ factor, are ready to be transferred off the GPU, and, its contribution block rows are ready to be assembled into its parent front. The scheduler builds a Pack Assembly task.
to perform this last operation. A front is finished when its rows of $R$ are transferred off
the GPU and its contribution block rows have been assembled into its parent.

Using CUDA events and streams, the Sparse QR Scheduler builds the list of tasks to
be completed by the next kernel launch while the previous kernel launch executes on
the GPU. This strategy affords us additional benefits. We are able to hide the latency
of memory traffic between the GPU device and the CPU host. We perform a transfer
of the $R$ factor in a non-blocking fashion by initiating an asynchronous memory trans-
er on a CUDA stream and marking an event to record when the transfer completes.
Furthermore, the $R$ factor may become available before factorization completes. This
occurs when the remaining factorization tasks involve only contribution block rows.

3.2. Staging for Large Trees

During symbolic analysis, the CPU may discover that the amount of memory required
to store the frontal matrices and assembly data on the GPU exceeds the total amount
of memory available to the device. When this occurs, we switch to a strategy where we
divide the assembly tree and perform the factorization in stages.

During symbolic analysis phase, in order to build the different stages, we traverse
the assembly tree following a postorder. We keep a running summation of the memory
required by each front. This is the summation of the number of entries in the front,
number of entries of its children, and number of entries in the original sparse input
matrix that are to be assembled into the front. We then also keep a list of stages to be
executed by the GPU. Each entry in the staging list is an index into the postordered
list. A new stage is created whenever the next front in the postorder would exceed the
memory limitation of the GPU.

During factorization phase, in order to execute a staged sparse factorization, we use
the CPU-based Sparse QR Scheduler for each stage. We transfer relevant values from
the original input problem and assembly mappings. We also allocate space on the GPU
for each front participating in the stage. Then, we invoke the Sparse QR Scheduler for
that stage. Fronts whose parents are in subsequent stages are flagged. This signals
to the Sparse QR Scheduler to bypass the Pack Assembly phase for these fronts. Such
fronts are roots of the subtrees illustrated in Figure 6.

When crossing staging boundaries, the contribution block of these fronts must be
marshaled into the next stage. We perform this marshaling at the end of a stage; when pulling rows of $R$ from the GPU, we also pull these contribution blocks into a
temporary location in CPU memory. As we build the data for the next stage, we send
these contribution blocks back to the GPU. When invoking the Sparse QR Scheduler for
the next stage, we flag fronts whose only data is contribution blocks. Those fronts
begin factorization at the Pack Assembly phase, as illustrated in Figure 7. In the figure,
fronts with no children have been activated and performing either Pack Assembly, if
the front was in stage 1, or S-Assembly, if it is new to this stage. Children performing
Pack Assembly are identified as yellow leaves, and children performing S-Assembly
are identified as light blue leaves.

3.3. Breaking the factorization into a sequence of GPU kernel launches

Now that the overall structure of the multifrontal tree has been described, we describe
in this section how we factorize multiple fronts within a tree in parallel, using a se-
quence of kernel launches on the GPU.

Our execution model uses a master-slave paradigm between CPU and GPU. On the
one hand, for each kernel launch, the CPU builds a list of tasks, sends the list to the
GPU, synchronizes the device, and launches the kernels. Although GPU instructions
exist for atomic operations and intra-SM thread synchronization, GPU devices offer
poor support for inter-SM synchronization. Thus, we construct the list of tasks such
that they have no dependencies between them at all. On the other hand, for each kernel launch, the GPU receives the list of tasks from the CPU and performs the operations described by each task.

Our kernel implementation is monolithic in the sense that the GPU executes the same global function for every task. However, every task starts by inspecting the task
descriptor data structure to identify its type, and thus, to select the appropriate device function to execute. In this manner, a single kernel launch computes the results for tasks in many different Factorize, Apply, and Assembly phases of the factorization pipeline simultaneously. This software design pattern is called the “uberkernel” [Tatarnov and Kharlamov 2009]. In this approach, one CUDA stream is used to execute different kinds of tasks. This contrasts with the alternative approach where multiple GPU streams are used, each one to execute a specific kind of task.

The factorization of the matrix may take several kernel launches to complete. In order to improve efficiency and reduce idle times, the CPU and GPU work asynchronously and in parallel, following a double buffered pipelined fashion and using the NVIDIA CUDA events and streams model. Specifically, while the GPU executes the list of tasks in a kernel launch, the CPU builds the list of tasks to be executed by the GPU on the next kernel launch. Two CUDA streams are used. While the GPU uses one stream, the CPU uses the other stream to send the next list of tasks asynchronously. Moreover, the CPU is responsible for synchronizing the device prior to launching the next kernel in order to ensure that the task data has arrived and that the previous kernel launch has completed.

A high-level view of our scheduling algorithm is shown in Figure 8. It provides a simplified diagram of how 8 frontal matrices can be factorized and assembled on the GPU in parallel. The black circles denote Factorization and Apply tasks, in which each the dense frontal matrices are factorized. Some frontal matrices are small enough to be factorized in a single kernel launch (nodes 1, 2, 5, 6, and 7), while others require multiple kernel launches (nodes 3, 4 and 8). Once a frontal matrix is factorized, its contribution block must be assembled into its parent (a Pack Assemble task), along with the input sparse matrix (an S-Assemble task). Both types of Assembly tasks are shown as A circles in the figure.
Note that there is no need for a barrier between levels of the assembly tree in Figure 8. One option for factorizing these frontal matrices would be to factorize nodes 1, 3, 5, 6, and 7 first, followed by 2 and 8, and so on. We do not use this approach since it would limit parallelism. For example, frontal matrix 3 is large enough to require many kernel launches, and while it is being factorized, both nodes 1 and 2 can be completed. Likewise, node 8 can start before node 3 finishes. This strategy enables us to reduce the number of kernel launches required to factorize the entire sparse matrix.

3.4. Factorizing dense frontal matrices via the Bucket Scheduler

We introduce a novel method for computing the QR factorization of a dense rectangular matrix. The method is well-suited for the factorization on GPU of the many dense frontal matrices that arise in a sparse multifrontal QR factorization.

The algorithm partitions the fronts into square submatrices that we refer to here as tiles. All the tiles in a row form a row tile, and row tiles are placed in buckets corresponding to their leftmost nonzero tile. The parallel factorization of a frontal matrix is analogous to a multiplayer Mancala\textsuperscript{1} game with pits and stones. Let each stone in the game represent a row tile, and let each pit be a bucket. Factorizing a submatrix corresponds to selecting some stones from a pit, leaving one of the stones in the pit from which it came and shifting the remaining stones to the pit to the right. The single stone that stays behind corresponds to the triangular factor in a single tile, while the rest of the stones correspond to the tiles that have been zeroed out. To allow for many simultaneous players, a single player does not take all stones from a pit. The game is over (and the frontal matrix factorized) when each pit contains one stone. Each player in this game is a single task assigned to an SM on the GPU, and since there are many stones in many pits, there are many independent tasks that can be included in each kernel launch. The schedule is deterministic since it is constructed by a single CPU thread, while the actual tasks are performed in parallel by the GPU.

Our CPU-based dense QR scheduler is comprised of a data structure representing the factorization state of a frontal matrix together with an algorithm for scheduling

\textsuperscript{1}https://en.wikipedia.org/wiki/Mancala
tasks to be performed by the GPU. We call this algorithm and its data structure the bucket scheduler. Each frontal matrix has its own bucket scheduler.

The algorithm partitions the input matrix into 32-by-32 tiles. The choice of a tile size reflects the thread geometry of the GPU and the amount of shared memory that each SM can access.

All tiles in a single row are called row tiles, so that (for example) a single row tile in a 256-by-160 matrix consists of a submatrix of size 32-by-160. In our scheduler, we refer to a row tile by a single integer, its row tile index. In contrast, a column tile is just a single tile, so one row tile in a 256-by-160 matrix consists of a 32-by-160 submatrix, containing 5 column tiles. The leftmost column tile in a row tile refers to the nonzero column tile with the least column tile index. In a row tile, all column tiles to the left of the leftmost column tile are all zero. Each row tile has a flag indicating whether or not its leftmost column tile is in upper triangular form. The goal of the QR factorization is to reduce the matrix so that the kth row tile has a leftmost column tile k in upper triangular form.

All 32 rows in a row tile are contiguous. A set of two or more row tiles with the same leftmost column tile can be placed in a bundle, which is a group of row tiles to be operated on by a single task on the GPU. The bundle corresponds to a set of stones picked up by a single player in the Mancala game. The row tiles in a bundle need not be contiguous. The bundle size is chosen based on the shared memory size of the GPU. For example, the NVIDIA C2070 has 64KB of shared memory, which corresponds to exactly 6 tiles. However, each tile in shared memory needs to be padded with an extra column to elimination bank conflicts, so only 5 tiles can be held. Our block Householder update kernel needs 3 tiles for V and T and two tiles for a workspace C, to perform a 3-by-2 tile update on a submatrix of a single frontal matrix. Thus, the size of the Householder bundle is 3 tiles on the C2070 GPU. For other GPUs, our algorithm could use a different bundle size.

We place row tiles into column buckets, where row tile i with leftmost column tile j is placed into column bucket j. During factorization, row tiles move from their initial positions in the column buckets to the right until each column bucket contains exactly one row tile with its flag set to indicate that it is upper triangular.

The CPU is responsible for manipulating row tiles within bundles, filling a queue of work for the GPU to perform, and advancing row tiles across column buckets until exactly one row tile remains in each column bucket. Each round of factorization builds a set of tasks by iterating over the column buckets and symbolically manipulating their constituent row tiles.

All row tiles in a bundle have the same leftmost column tile, prior to factorization of the bundle. After factorization, the leftmost column tile of the topmost row tile is placed into upper triangular form, and the leftmost column tile of the remaining row tiles are all zeroed out. The bundle now represents a set of row tiles to which a block Householder update must be applied to all column tiles to the right of the leftmost column tile of the bundle.

We iterate over the column buckets and for each column bucket and perform the operations described below, building a set of tasks to be executed by the GPU at each kernel launch, illustrated in Figure 9. Each image in the figure represents the tasks at each kernel launch and is color-coded by bundle. Gray tiles are unmodified by their respective kernel launches. White tiles are finished.

(1) **Generate bundles and build block Householder update tasks on the CPU:**

Row tiles that are unassociated with a bundle become new bundles ready for factorization. Figure 9b illustrates this by grouping tiles into bundles of size 3 (red), 3 (magenta), and 2 (green). Factorize tasks are created for such bundles. Continuing
Fig. 9. Factorization in 12 kernel launches.

ACM Transactions on Mathematical Software, Vol. 1, No. 1, Article 1, Publication date: May 2016.
the Mancala analogy, there are 5 pits (buckets) in this game, and in this state of the factorization, pit 1 contains 6 stones (row tiles 1 through 6), pit 2 contains 2 stones (row tiles 7 and 8), and the other pits are empty. At this step, three players can play in parallel (red, magenta, and green).

(2) **Launch the kernel with its current set of non-uniform tasks:** Launch the GPU kernel and perform any queued Factorize, Apply, and Assembly tasks. Factorize tasks factorize the leftmost column tile in each bundle, and Apply tasks apply a block Householder update from a prior Factorize task in the previous kernel launch. The Assembly tasks push the contribution block from a frontal matrix into its parent, and is used only when the frontal matrix is factorized (not shown in Figure 9).

(3) **Advance the bundles on the CPU:** Next we advance the bundles, leaving the topmost row tile in upper triangular form, as shown in Figure 9c and Figure 9d for row tile 1 in column bucket 1, for example. These advancing bundles move to the next column bucket and represent a pending block Householder update from the previous factorization step. Figure 9c shows two stones (1 and 2) in the first pit. The second pit holds stones 2, 3, 5, 6, and 7. The third pit holds the 8th stone. For the next kernel launch, a Factorize task (cyan) will handle row tiles 1 and 4 in the first column bucket. The remaining tasks will apply the Householder updates for the red, green, and magenta tasks. Four Mancala players can play at the same time in Figure 9c; one is picking up the two stones in bucket 1 (cyan), while the other three are applying their Householder updates after moving their stones to the right (red, magenta, and green).

We continue performing the operations described above until only one upper triangular row tile appears in each column bucket, as shown in Figure 9n. In this state, each pit in the Mancala game holds a single stone. The matrix is factorized, the game is over, and there is no more work to be done to factorize the frontal matrix. The contribution block is now ready to be assembled into its parent.

### 3.5. Computational Kernels on the GPU

In this section, we provide details of the kernels required for the simultaneous dense QR factorization and assembly of multiple frontal matrices on the GPU.

The Factorize task factorizes the leading tiles of a bundle, producing a block Householder update (the $V$ and $T$ matrices) and an upper triangular factor $R$ in the top row tile. The Apply task uses the $V$ and $T$ matrices to apply the block Householder update to the remaining column tiles, to the right in this bundle.

Our tile size is selected to be a 32-by-32 submatrix, so that the row and column dimensions match the size of a GPU warp (32 threads). Six tiles can fit exactly into the 48K of shared RAM available each SM of a C2070 GPU, but with padding this drops to five tiles. The $V$ matrix is lower trapezoidal and $T$ is a single upper triangular tile, so three tiles are set aside for $V$ and $T$ (plus one row to avoid overlapping their diagonals). Three tiles are used for $V$, and the upper triangular part of its topmost tile (where $V$ is lower triangular) holds the matrix $T$. Two tiles hold a temporary matrix $C$.

#### 3.5.1. Factorize kernel

From a high-level perspective, we describe now the Householder QR factorization algorithm on an $m$-by-$n$ matrix $A$.

The factorize function shown below is a MATLAB implementation. The Factorize task implements it on the GPU.

```matlab
function [A V1 T] = factorize(A)
```

ACM Transactions on Mathematical Software, Vol. 1, No. 1, Article 1, Publication date: May 2016.
\[[m \ n] = \text{size} (A)\]
\[T = \text{zeros} (n)\]
for \(k = 1:n\)
\[\tau, v = \text{house} (A (k:m,k))\]
\[V1 (k) = v (1)\]
\[A (k+1:m,k) = v (2:end)\]
\[z = -\tau \cdot v' \cdot A (k:m,:)\]
\[A (k:m,k+1:n) = A (k:m,k+1:n) + v \cdot z (k+1:n)\]
\[T (1:k-1,k) = T (1:k-1,1:k-1) \cdot z (1:k-1)'
\]
\[T (k,k) = \tau\]
end

The \textit{factorize} function overwrites \(A\) with the factor \(R\) and the Householder vectors \(V\). Simultaneously, it creates \(T\) for the subsequent block Householder update and a vector \(V1\) that holds the diagonal of \(V\). The \textit{house} function computes the Householder vector \(v\) and coefficient \(\tau\) to annihilate the \(k\)th column of \(A\).

A key feature illustrated by the \textit{factorize} function is the merging of some of the work for the \(k\)th Householder update with the construction of the \(T\) matrix. Specifically, these two operations are merged into the single matrix-vector multiply computation of the \(z\) vector in the statement \(z = -\tau \cdot v' \cdot A (k:m,:)\). Some threads will own parts of \(A\) overwritten with \(V\) (in columns 1 to \(k\)), and these take part in the construction of the \(k\)th column of \(T\). Other threads hold parts of \(A\) that must be updated by the \(k\)th Householder vector. This way, all threads of the SM are kept busy, making useful progress in the computation, at the same time.

From a mid-level perspective, we describe now the layout of the different data structures on GPU.

The \textit{Factorize} task takes a (rectangular) \(A\) matrix as an input, and produces the (upper triangular) \(R\) matrix as a result, and the (lower trapezoidal) \(V\) and (upper triangular) \(T\) matrices as an output. The \(A\) matrix is the set of leftmost column tiles of a given bundle. These tiles are non-contiguous in memory. The upper right triangular part of the topmost column tile of \(A\) is overwritten by \(R\). The remaining bottom column tiles of \(A\) are overwritten by the bottom column tiles of \(V\). The lower left triangular portion of the topmost tile of \(V\) is stored together with \(T\) in a combined structure we denote as the \(VT\) tile. Because both \(V\) and \(T\) contain diagonal values, the resulting memory space is a 33-by-32 tile with \(V\) offset by 1. The \(V\) and \(T\) matrices are saved by the \textit{Factorize} task and remain in memory until they get used by the \textit{Apply} task in a next GPU kernel launch, for the block Householder update of the remaining columns in the bundle. At that point, the \(VT\) tile space is freed to hold another \(VT\) tile, from another bundle in the current front or in another front being factorized at the same time.

From a low-level perspective, we describe now the implementation details on the GPU.

This description assumes a bundle of three tiles and a kernel launch with 384 threads per task, but we have other kernels for different bundle sizes.

(1) \textbf{Load} \(A\) \textbf{from global memory}. All 384 threads in the task cooperate to load the bundle’s tiles from global memory (the \(A\) matrix of size \(m\)-by-\(n\)) into a single shared memory array of size \(m\)-by-(\(n + 1\)) where \(m = 96\) and \(n = 32\). No computation is performed while \(A\) is being loaded. After \(A\) is loaded, each thread loads into register 8 entries of \(A\) along a single column for which it is responsible. It keeps these entries in register for the entire factorization. We call this 8-by-1 submatrix operated on by a single thread a \textit{bitty block}. 

ACM Transactions on Mathematical Software, Vol. 1, No. 1, Article 1, Publication date: May 2016.
(2) **Compute \( \sigma \) for the first column**, where \( \sigma = \sum (A_{2:m,1})^2 \) (where \( 2 : m \) denotes \( 2 \ldots m \)). This computation is the bulk of the work for finding the Householder vector, and is composed of two reduction operations. First, the 12 threads responsible for the first column of \( A \) compute the sum of squares using an 8-way fused multiply-add reduction in register memory, saving the final result into shared memory. Threads in the thread block synchronize to ensure they have all finished the first phase before entering the second phase of the reduction. We designate the first thread in the thread block to be the *master thread*. The master thread completes the computation with a 12-way summation reduction reading from shared memory into register memory. The master thread retains \( \sigma \) in register during the factorization loop.

(3) **The main factorization loop** iterates over the columns of \( A \), performing the following operations (a) through (f) in sequence.

(a) **Write the \( k \text{th} \) column of \( A \) back into shared memory** The threads responsible for the \( k \text{th} \) column write their \( A \) values from register back into shared memory. The SM then synchronizes all 384 threads before proceeding, maintaining memory consistency. Once the diagonal value is computed, the \( k \text{th} \) column becomes the \( k \text{th} \) Householder vector \( v \). Additionally, values above the diagonal are the \( k \text{th} \) column of \( R \). In the *factorize* MATLAB function, this step roughly corresponds to the step \( A(k+1:m,k) = v(2:end) \).

(b) **Compute the \( k \text{th} \) diagonal.** This step finalizes the construction of the \( k \text{th} \) Householder vector. The master thread is responsible for computing the \( k \text{th} \) diagonal entry of \( R \), the \( k \text{th} \) diagonal entry of \( V \), and \( \tau \): \( s = \sqrt{a_{kk}^2 + \sigma} \), \( v_{kk} = a_{kk} - s \) if \( a_{kk} \leq 0 \) and \( -\sigma/a_{kk} + s \) otherwise, and \( \tau = -1/sv_{kk} \). If \( \sigma \) is very small, the square root is skipped, and \( v_{kk} \) along with \( \tau \) are set to 0. Because all threads will need \( v_{kk} \) and \( \tau \), the remaining threads synchronize with the master thread.

(c) **Compute an intermediate \( z \) vector.** All threads cooperate to perform a matrix-vector multiply \( z = -\tau v \text{T} A_{k:m,1:n} \), which is used to compute the \( V \) and \( T \) matrices, where \( v \) is the Householder vector, held in \( A_{k:m,k} \). To compute \( z \), each thread loads the entries of the \( v \) vector it requires from shared memory into register memory, from \( A_{k:m,k} \). The thread’s bitty block of \( A \) is already in register (the 8 entries of \( A \) that the thread operates on).

The calculation is done in two parts. The first part is illustrated in Figure 10, where each thread performs an 8-way partial dot product reduction using fused multiply-adds in register memory. The threads store the partial result in a 12-
Fig. 11. Householder update: \( A(k:m,k+1:n) = A(k:m,k+1:n) + v \cdot z(k+1:n) \)

Fig. 12. Construct \( k^{th} \) column of \( T \), with: 
\[
T(1:k-1,k) = T(1:k-1,1:k-1) \cdot z(1:k-1)'
\]

by-32 region of shared memory. The threads synchronize to guarantee that they have completed the operation before proceeding with the second phase of the calculation. The second phase of the calculation involves only a single warp. This warp performs the final 12-way summation reduction into shared memory, completing the calculation of \( z \).

(d) **Householder update of \( A \) in register memory**, illustrated in Figure 11. All threads responsible for columns to the right of the \( k^{th} \) column of \( A \) participate in updating \( A \) by summing values with the outer product \( A_{k:m,k+1:n} = A_{k:m,k+1:n} + v_z(k+1:n) \). Threads involved in the outer product computation already have \( v \) in register memory, and they need only load \( z \) from shared memory once to update their values of \( A \). Each thread needs to load a single value of \( z \), since each bitty block is 8-by-1, in a single column of \( A \).

(e) **Compute the next \( \sigma \) value.** Some threads participating in updating \( A \) in register memory may also begin to compute the next \( \sigma \) value if they are responsible for the \((k+1)^{st}\) column of \( A \). These threads participate in computing \( \sigma \), and the process is the same as the computation of \( \sigma \) for the first column.

(f) **Construct the \( k^{th} \) column of \( T \), with** 
\[
T_{1:k-1,k} = T_{1:k-1,1:k-1} \cdot z_{k-1:k-1}^T
\]

This step is illustrated in Figure 12. Threads 1 to \( k-1 \) are assigned to compute the \( k^{th} \) column of \( T \), where the \( i^{th} \) thread performs the inner product to compute \( t_{ik} \). Threads load values of \( T \) and \( z \) from shared memory, accumulating the result in register memory. Finally, the participating threads each write their scalar result \( t_{ik} \) from register memory into shared memory. The master thread writes \( t_{kk} = \tau \).

(4) **Store \( A, V, \) and \( T \) back into global memory.** All 384 threads in the task cooperate to store the bundle’s tiles back into global memory. Since the first tile of \( V \)
and $T$ are held in a single VT tile in global memory, they are stored together to maintain coalesced global memory transactions.

Once the VT tile is stored, the three tiles that hold $A$ are stored back into global memory in the frontal matrix being factorized. The first tile of $A$ is the upper triangular matrix $R$, and the remaining tiles are the second and third tiles of the Householder vectors, $V$.

3.5.2. Apply kernel. Each Apply task involves a bundle, an originating column tile, a column tile range, and the location of the VT tile. The GPU loads the VT tile and iterates over the column tile range performing the block Householder update, (1) $C = V^T A$, (2) $C = T^T C$, and (3) $A = A - VC$.

Since the $V$ and $T$ matrices are used repeatedly, and since $V$ is accessed both by row and column order ($V$ and $V^T$), they are loaded from global memory by the SM and held in shared memory until the Apply task completes. The temporary $C$ matrix is also held in shared memory or register. The $A$ matrix remains only in global memory, and is staged into a shared memory buffer and then into register, one chunk at a time. The algorithm is as follows:

— Load $V$ and $T$. All 384 threads in the task cooperate to load the $V$ and $T$ matrices from global memory into a single shared memory array of size 97-by-32. Since the first tile of $V$ and $T$ are held in a single VT tile in global memory, they are loaded together to maintain coalesced global memory accesses. No computation is performed while $V$ and $T$ are being loaded.

— Apply the block Householder: $A = A - VT^T V^T A$. The $A$ matrix is 3-by-$t$ tiles in size in global memory, and represents a portion of the frontal matrix being factorized. Since $V$ and $T$ take up three tiles of shared memory, two tiles remain for a temporary matrix ($C$) required to apply the block Householder update. Registers also limit the size of $C$ and the submatrix of $A$ that can be operated on. If held in register, each thread can operate on at most a 4-by-4 submatrix of $A$ or $C$ (its bitty block). With 384 threads, this results in a submatrix of $A$ of size 96-by-64, or 3-by-2 tiles. The same column dimension governs the size of $C$, which is 2-by-1 tiles in size. Thus, the $t$ column tiles of $A$ are updated two at a time. Henceforth, to simplify the discussion, $A$ refers to the 96-by-64 submatrix (3-by-2 tiles) updated in each iteration across the $t$ column tiles. The block update is computed in three phases as (1) $C = V^T A$, (2) $C = T^T C$, and (3) $A = A - VC$, as follows:

1. Load $A$ and compute $C = V^T A$. This work is done in steps of 16 rows each (a halftile), in a pipelined manner, where data for the next halftile is loaded from global memory into shared, while the current halftile is being computed. This enables the memory / computation overlap required for best performance. The $C$ matrix is held in register, so the 2 tiles of shared memory (for $C$) are used to buffer the $A$ matrix. This 32-by-64 matrix is split into two buffers $B_0$ and $B_1$, each of size 16-by-64 (two halftiles).

All threads prefetch the first halftile ($p = 0$) into register, which is the topmost 16-by-64 submatrix of $A$. This starts the pipeline going. Next, $C = V^T A$ is computed across six halftiles, one halftile ($p$) at a time:

\[
\begin{align*}
\text{for} \quad p &= 1 \text{ to } 6 \\
\text{a. Write this halftile ($p$) of $A$ from register into shared buffer $B_{p \mod 2}$.} \\
\text{b. syncthreads.} \\
\text{c. Prefetch the next halftile ($p + 1$) of $A$ from global to register.} \\
\text{d. Compute $C = V^T A$, where $A$ is in buffer $B_{p \mod 2}$.} \\
\end{align*}
\]
In step (b), all threads must wait until all threads reach this step, since there is a dependency between steps (a) and (d). However, steps (c) and (d) can occur simultaneously since they operate on different halftiles. In step (d), each thread computes a 4-by-2 bitty block of $C$, held in register for phases 1 and 2 (only the first 256 threads do step (d); the other 128 threads remain idle and are only used for memory transactions in this phase).

The global memory transactions for a warp are scheduled in step (c), but the warp does not need to wait for them to be completed before computing step (d) (they are not needed until step (d) of iteration $p+1$). Likewise, no synchronization is required between step (d) of iteration $p$ and step (a) of the next iteration $p+1$. Since steps (c) and (d) (for iteration $p$) can overlap with step (a) (for iteration $p+1$), this algorithm keeps all parts of the SM busy at the same time: computation (step (d)), global memory (step (c)), and shared memory (steps (a) and (d)).

(2) Compute $C = T^T C$. All matrices are now in shared memory. Each thread operates on the same 4-by-2 bitty block of $C$ it operated on in phase 1, above, and now writes its bitty block into the two tiles of shared memory. These are no longer needed for the buffer $B$, but now hold $C$ instead. Only the first 256 threads take part in this computation.

(3) Compute $A = A - VC$, where $V$ and $C$ are in shared memory but $A$ remains in global. The $A$ matrix had already been loaded in from global memory once, in phase 1, but it was discarded since the limited shared memory is already exhausted by holding $V$, $T$ and the $C/B$ buffer. Each of the 384 threads updates a 4-by-4 bitty block of $A$.

The layout of the bitty blocks of $A$ and $C$ is an essential component to the algorithm. Proper design of the bitty blocks avoids bank conflicts and ensures that $A$ is accessed with coalesced global memory accesses. Both $A$ and $C$ bitty blocks are spread across the matrices. They are not contiguous submatrices of $A$ and $C$. The $C$ matrix is 32-by-64 and is operated on by threads 0 to 255. Using 0-based notation, the 4-by-2 bitty block for thread $i$ is defined as

$$C[i] = \begin{bmatrix} C(i \mod 8),((i/8)] & C(i \mod 8),(32+[i/8]) \\ C(8+i \mod 8),([i/8]) & C(8+i \mod 8),(32+[i/8]) \\ C(16+i \mod 8),([i/8]) & C(16+i \mod 8),(32+[i/8]) \\ C(24+i \mod 8),([i/8]) & C(24+i \mod 8),(32+[i/8]) \end{bmatrix}$$

where $c_{0,0}$ is the top left entry of $C$. For example, the bitty blocks of threads 0 and 1 are, respectively:

$$C[0] = \begin{bmatrix} c_{0,0} & c_{0,32} \\ c_{8,0} & c_{8,32} \\ c_{16,0} & c_{16,32} \\ c_{24,0} & c_{24,32} \end{bmatrix}, \quad C[1] = \begin{bmatrix} c_{1,0} & c_{1,32} \\ c_{9,0} & c_{9,32} \\ c_{17,0} & c_{17,32} \\ c_{25,0} & c_{25,32} \end{bmatrix}$$

The 4-by-4 bitty block of $A$ for thread $i$ is defined very differently than the $C$ bitty block, where $A[i] = \begin{bmatrix} a((i/16),(i \mod 16) & \ldots & a((i/16),(48+i \mod 16) \\ a(24+i/16),(i \mod 16) & \ldots & a(24+i/16),(48+i \mod 16) \\ a(48+i/16),(i \mod 16) & \ldots & a(48+i/16),(48+i \mod 16) \\ a(72+i/16),(i \mod 16) & \ldots & a(72+i/16),(48+i \mod 16) \end{bmatrix}$

so that thread 0 owns $a_{0,0}$ and thread 1 owns $a_{0,1}$. When used in our algorithm, these layouts of the $C$ and $A$ bitty blocks ensure that all global memory accesses are coalesced, that no memory bank conflicts occur, and that no significant register spilling occurs in our kernels.

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With a 4-by-4 bitty block for $A$, each thread loads in 8 values from shared memory (a 4-by-1 column vector of $V$ and a 1-by-4 row vector of $C$), and then performs 32 floating point operations (a rank 1 outer product update of its 4-by-4 bitty block). This gives a flops per memory transfer ratio of 4, which is essential because the floating point units for the C2070 GPU are 4 times faster than register bandwidth. The 4-by-2 bitty block for $C$ requires 6 loads for 16 operations, a ratio of $16/6 = 2.67$. Since this is less than 4, it is sub-optimal, but unavoidable in the context of the entire block Householder update.

3.5.3. Assembly Kernels. In addition to the compute kernels used in the dense QR factorization, sparse QR factorization employs two kernels responsible for data movement:

— **S-Assembly** refers to scattering values from the permuted sparse input matrix, $S$, into the dense frontal matrices residing on the GPU. The CPU packs all $S$ entries for fronts within a stage into a list of index-value tuples, and describes to the GPU where each front can find its $S$ entries. The value is copied within global memory to a frontal matrix at the location referred to by the index field of the tuple. The data movement is embarrassingly parallel since multifrontal QR factorization relies on concatenation of the children contribution blocks. This is in contrast to multifrontal LU or Cholesky factorization, where the contribution blocks of multiple children must be summed, not concatenated.

We select a granularity with which to build S-Assembly tasks. In our implementation, each thread is responsible for moving 4 values into position. S-Assembly may occur concurrently with children pushing their contribution blocks into the front.

— **Pack Assembly** refers to scattering values from a front's contribution block into its parent. The CPU builds and sends two maps to the GPU that describe the correspondence between a front's row and column indices to its parent's row and column indices. We call these two maps $Rimap$ and $Rjmap$, respectively. When a front completes its factorization step, the values in its contribution block are copied into its parent front. The CPU describes to the GPU where the front's contribution block begins, where its parent resides in GPU memory, the number of values to copy, and the location of $Rimap$ and $Rjmap$. The GPU reads $Rimap$ and $Rjmap$ into shared memory and uses shared memory as a cache for fast index translations. The data movement is embarrassingly parallel as with S-Assembly, and we select a granularity that best suits GPU shared memory limits per streaming multiprocessor. We select a maximum Pack Assembly tile size of 2048 entries of $Rimap$ and $Rjmap$.

4. EXPERIMENTAL RESULTS

In this section, we start by describing the experimental environment in Section 4.1 and end by discussing the performance of our algorithms in Section 4.2.

4.1. Experimental environment

Tables I and II describe the experimental environment. Table I describes the characteristics of the single shared-memory systems we used, namely: **GPUS2**, equipped with an AMD Opteron CPU and an NVIDIA C2070 (Fermi) GPU; **Backslash**, equipped with an Intel Xeon CPU and eight NVIDIA K40m (Kepler) GPUs, although only one GPU is used. Table II describes the performance of both CPU and GPU of the two systems, using different relevant performance metrics.

All results we present are in double precision. NVIDIA provides a cuBLAS for dense matrix operations such as matrix-matrix multiply (DGEMM); see https://developer.nvidia.com/gpu-accelerated-libraries. Both of the cuBLAS and MAGMA libraries obtain high performance for the dense QR factorization of a sin-
gle dense matrix, but they are not suited to factorizing a set of inter-related dense frontal matrices of very different sizes, which arises in the sparse case.

Table I. Computers description

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<th>GPUS2</th>
<th>Backslash</th>
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Table II. Computers performance

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<td>QR</td>
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<td>QR (MAGMA)</td>
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4.2. Performance results

We provide now the performance results of our dense and sparse QR factorizations. Although they are provided for both the GPUS2 and Backslash systems, the emphasis here is on the former system, as the GPU kernels we have presented in this paper are customized for the C2070 GPU. The results on the later system are provided as a mean of comparison, in order to show the gains in performance obtained by using a newer generation of GPU architectures, the K40m.

We measured the performance of each of our compute kernels individually. Apply tasks are able to achieve up to 183.3 GFlops, when we flood the GPU with an unlimited number of them to keep all SMs busy. Similarly, Factorize tasks are able to achieve up to 23.62 GFlops. When a frontal matrix is small enough that it can be factorized by a single task, the VT tile need not be computed. In this case, the factorize tasks are able to achieve up to 34.80 GFlops on a 72-by-64 frontal matrix. Factorize tasks suffer from a hefty initial serial fraction computing $\sigma$ for the first column.

We also measured the performance of QR factorization for dense matrices, presented in Tables III and IV. In the tables, Canonical GFlops reflects the Golub and Van Loan flop count for factoring dense matrices [Golub and Van Loan 2012], and GPU GFlops is based on the number of flops actually performed by the GPU device. The algorithm is able to achieve up to 31.83% of the Tesla C2070’s peak theoretical double-precision performance.
We compared our GPU-accelerated sparse QR with Davis' CPU-only SuiteSparseQR on 624 problems from the SuiteSparse Matrix Collection [Davis and Hu 2011]. SuiteSparseQR uses LAPACK for panel factorization and block Householder applies while our GPU-accelerated code uses our GPU compute kernels to accomplish the same.

In Table V, we describe a sample problem set representing a variety of domains. Table VI shows the results for these six matrices on our CPU and our GPU, and the relative speedup obtained on the GPU. Intensity refers to arithmetic intensity, the number of floating point operations required to factorize the matrix divided by the amount of memory (in bytes) required to represent the matrix. The flop count (fl.) is the number of floating point operations needed to factorize the matrix, in billions (a canonical count, not what the GPU actually performs). The total time and GFlop rate includes all computation (including the time taken by the CPU to construct the schedule) and all CPU-GPU data transfers.

Figure 13 shows the speedup of our GPU-accelerated code over the SuiteSparseQR code as a function of arithmetic intensity for all test matrices, in a logarithmic scale. The arithmetic intensity of a problem is known prior to the numerical factorization, since the total flop count and memory usage are metrics computed in the analysis phase. If this ratio is low (less than 10, say), the GPU can be skipped and the entire work can be done on the CPU. Problems with a high arithmetic intensity are also...
those taking the most time and flops to factorize, so this strategy will only relegate small matrices to the CPU, where their tiny factorization time is not critical.

We already use a similar strategy in the MATLAB backslash, \( x = A \backslash b \), which relies on our sparse Cholesky solver CHOLMOD (Algorithm 887) [Davis and Hager 2009; Chen et al. 2008]. In CHOLMOD, we measure the arithmetic intensity as the ratio of total flop count over the number of nonzeros in the factor (with between 8 to 12 bytes per nonzero, depending on the matrix). If this metric is over 40, then CHOLMOD automatically uses a supernodal factorization that exploits the BLAS. If the ratio is less than 40, a non-supernodal up-looking factorization that does not use the BLAS is almost always faster, and we automatically use that method. The up-looking solver is the same method (but different code) as the simple sparse Cholesky solver in CSparse [Davis 2006] and Algorithm 849 [Davis 2005]. This algorithmic choice is transparent to the MATLAB user. The value of 40 for this metric is not directly comparable to the flops/byte metric in Figure 13, but it corresponds to about 4 or 5 for the ratio used in that figure, depending on the matrix.

As a result of this strategy, the matrices in Figure 13 with computational intensity less than about 50 can use the CPU, and the slowdown from the GPU on these small problems can be entirely avoided. Future tests on many different kinds of GPUs are needed to determine the best automatic threshold to use for any given GPU.

Table VII summarizes the distribution of the performance (GPU speedup over the CPU) for four different ranges of arithmetic intensity that were plotted in Figure 13. The table excludes matrices with an intensity below 10 flops/byte. Many problems experience significant speedup of up to 11x over the CPU-based method. We obtain a median speedup 5x for large problems, which are those with high arithmetic intensity (100 flops/byte or higher). The speedups shown in Figure 13 and summarized in Table VII can actually exceed the speedup of a dense matrix multiplication (DGEMM) on the GPU as compared to the CPU (Table II). This is because our bucket-scheduler based QR factorization on the GPU is entirely different than our prior sparse QR factorization on the CPU. Speedup is limited by two factors:

1. **Available parallel flops:** Dense QR factorization offers \( O(n^3) \) flops for \( O(n^3) \) memory storage. As arithmetic intensity increases, the algorithm is able to exploit more parallelism than the CPU-based method. However, for small problems such as circuit_2 in Table V, the algorithm is unable to exploit enough parallelism.
Table VII. GPU speedup as a function of arithmetic intensity

<table>
<thead>
<tr>
<th>computational intensity</th>
<th>number of matrices</th>
<th>speedup</th>
<th>Backslash</th>
<th>speedup</th>
</tr>
</thead>
<tbody>
<tr>
<td>low</td>
<td>high</td>
<td>min</td>
<td>median</td>
<td>max</td>
</tr>
<tr>
<td>10</td>
<td>30</td>
<td>0.5</td>
<td>2.1</td>
<td>8.1</td>
</tr>
<tr>
<td>30</td>
<td>100</td>
<td>0.7</td>
<td>3.8</td>
<td>10.6</td>
</tr>
<tr>
<td>100</td>
<td>300</td>
<td>1.3</td>
<td>5.2</td>
<td>10.6</td>
</tr>
<tr>
<td>300</td>
<td>2206</td>
<td>2.3</td>
<td>5.1</td>
<td>11.4</td>
</tr>
</tbody>
</table>

Thus, the time to factorize for small problems is dominated by memory transfer costs.

(2) **Hardware resources on the GPU**: Current GPU devices offer several cores arranged into SMs along with small amounts of fast shared memory per SM. Our algorithm is designed to flood the GPU device with many parallel tasks. However, as problem size grows with arithmetic intensity, we reach a performance asymptote as the amount of available GPU hardware resources begins to limit the performance of our algorithm.

On the CPU, SuiteSparseQR can exploit two forms of shared-memory parallelism: parallelism within the BLAS and explicit parallelism via Intel's Threaded Building Blocks (TBB). With TBB, the tree is partitioned into subtrees that are given to TBB tasks. By default, only BLAS-level parallelism is used because these two methods of parallelism can conflict. All our results presented so far use no TBB parallelism when comparing the CPU and GPU algorithms. The following results illustrate why this choice was made. As discussed in our prior paper, [Davis 2011], selecting the right number of threads for each form of parallelism is very problem dependent. The wrong choice can lead to a reduction in performance. To illustrate this, Table VIII reports the results of an experiment on Backslash with 24 CPU cores. We tested every combination of TBB and BLAS threads (1 to 24 for each option) for a total of $24 \times 24 = 576$ runs per matrix, and compared the run time with the SuiteSparseQR default (with no TBB parallelism and 24 BLAS threads). The best and worst relative speedups are shown in Table VIII (where a speedup of less than one means the method is slower than the default settings). In contrast, speedup on the GPU is easy to predict. If the arithmetic intensity exceeds a specific threshold (about 50 flops/bytes on Backslash), then the GPU is always faster. This is not the case for TBB versus BLAS parallelism on the CPU cores. Table VIII shows no particular trend as to which form of parallelism is best. It does not depend on arithmetic intensity. Furthermore, the potential benefit for using TBB is less for the larger matrices in Table VIII.

<table>
<thead>
<tr>
<th>problem</th>
<th>speedup</th>
<th>best case vs default</th>
<th>BLAS threads</th>
<th>worst case vs default</th>
<th>TBB threads</th>
<th>BLAS threads</th>
</tr>
</thead>
<tbody>
<tr>
<td>circuit_2</td>
<td>1.75</td>
<td>3</td>
<td>3</td>
<td>0.21</td>
<td>2</td>
<td>23</td>
</tr>
<tr>
<td>lp_cre_d</td>
<td>3.14</td>
<td>11</td>
<td>6</td>
<td>0.28</td>
<td>20</td>
<td>24</td>
</tr>
<tr>
<td>EternityII_A</td>
<td>3.49</td>
<td>24</td>
<td>5</td>
<td>0.31</td>
<td>10</td>
<td>22</td>
</tr>
<tr>
<td>olesnik0</td>
<td>2.80</td>
<td>3</td>
<td>7</td>
<td>0.17</td>
<td>18</td>
<td>24</td>
</tr>
<tr>
<td>lp_nug20</td>
<td>1.35</td>
<td>2</td>
<td>10</td>
<td>0.20</td>
<td>7</td>
<td>1</td>
</tr>
<tr>
<td>ch7-8-b3</td>
<td>1.08</td>
<td>19</td>
<td>20</td>
<td>0.13</td>
<td>3</td>
<td>1</td>
</tr>
</tbody>
</table>

5. FUTURE WORK

QR factorization is representative of many other sparse direct methods, with both irregular coarse-grain parallelism and regular fine-grain parallelism, and these methodologies will be very relevant for other methods.
Further parallelism is possible by extending our staging strategy to split the fronts for a stage across multiple GPU devices. The CPU could be used as an additional compute device to factorize some of the fronts in parallel with the GPU. Finally, for distributed memory systems, extending the CPU-based scheduler using MPI would allow for multiple GPU-accelerated systems to participate in the factorization.

There are many detailed aspects of the interplay between the GPU kernels, the algorithms, and the GPU architecture. As GPUs change we need to be able to adapt by changing the thread layout, the tile sizes, and many other low-level algorithmic details. We intend to create a suite of kernels that can be used in an auto-tuning framework to address this issue.

Finally, we intend on providing a MATLAB interface to our GPU-accelerated algorithm via the new MexCUDA MATLAB function for compiling GPU kernels for use in MATLAB.

6. RELATED WORK

[Anderson et al. 2010], [Demmel et al. 2008; 2012], and [Dongarra et al. 2013] consider how to exploit the orthogonal properties of QR factorization to reduce communication costs in parallel methods for dense matrices. Our bucket scheduler is an extension of this idea. Prior methods do not consider the sparse case, nor the staircase-form of our frontal matrices. They do not consider multiple factorizations and multiple assembly operations simultaneously active on the same GPU, as we must do in our sparse QR.

In an earlier work, [Davis and Davidson 1988] present a parallel sparse LU factorization algorithm with a non-deterministic pairwise pivoting strategy (PSolve). That method is analogous to the bucket scheduler presented here, except that in PSolve, each tile is a single row of the matrix, the bundle size is always 2, and each thread selects work from the buckets on their own in a non-deterministic fashion. The bucket scheduler for our sparse QR factorization is deterministic; the same matrix always generates the same set of kernel launches for its factorization.

[Krawezik and Poole 2009], [Lucas et al. 2010], [Pierce et al. 2009], [Vuduc et al. 2010], and [George et al. 2011] have worked on multifrontal factorization methods for GPUs. All five methods exploit the GPU by transferring one frontal matrix or supernode at a time to the GPU and then retrieving the results. The assembly operations are done in the CPU. [Sao et al. 2014] focuses on a distributed-memory approach with multiple CPUs and GPUs. On a single GPU they pack multiple GEMM’s together into a single BLAS kernel, for the outer product update with a single supernode.

The work of [Hogg et al. 2014] is most similar to the work present here. They present a multifrontal factorization method for symmetric indefinite matrices that also allows all frontal matrices to be factorized on the GPU. Their work differs from our sparse QR factorization in several ways. The primary difference is that their algorithm considers parallelism according to levels in the assembly tree, whereas our bucket scheduling method allows for parallelism across different levels of the tree.

In our left-looking supernodal sparse Cholesky factorization, [Rennich et al. 2014], we operate on many supernodes at the same time, by batching together all the small supernodes in a single level of a subtree of the elimination tree. The batching method is used at lower levels of the tree. We do not mix levels, as we do in the current work presented here. At higher levels, we operate on a single supernode at a time, and parallelize the update of a supernode from all its descendants.

[Aguillo et al. 2014] show how a runtime system can be used to effectively implement a multifrontal sparse QR factorization on a heterogeneous system. Their method relies on both the CPUs and the GPUs to perform the numerical factorization. The runtime system may run any given task on either a multicore CPU or on a GPU, depending on the task characteristics.
For additional background, [Davis et al. 2016] provide an extensive survey of sparse direct methods, including sparse QR factorization.

7. SUMMARY
In this paper, we presented a novel sparse QR factorization method tailored for use on GPU-accelerated systems. The algorithm is able to factorize multiple frontal matrices simultaneously, while limiting costly memory transfers between CPU and GPU.

The algorithm uses the master-slave paradigm where the CPU serves as the master and the GPU as the slave. We extend the Communication-Avoiding QR factorization [Demmel et al. 2012] strategy using our bucket scheduler, exploiting a large degree of parallelism and reducing the overall number of GPU kernel launches required to factorize the problem.

The algorithm uses the überkernel design pattern, allowing many different tasks for many different fronts to be computed simultaneously in a single kernel launch. Additionally, the algorithm schedules two flavors of assembly tasks that move data between memory spaces on the GPU. These assembly tasks are responsible for transferring data from a packed input into frontal matrices prior to factorization as well as transferring data from child fronts to parent fronts. As fronts are factorized, their rows of $R$ are asynchronously transferred off the GPU using CUDA events and streams.

For large sparse problems whose frontal matrices cannot simultaneously fit on the GPU, our algorithm examines the frontal matrix assembly tree and divides the fronts into stages of execution. The algorithm then moves data in stages to the GPU, factorizes the fronts within the stage, and transfers the results off the GPU. Contribution blocks are then passed back to the GPU, ready for push assembly.

For large sparse matrices, the GPU-accelerated code offers up to 11x speedup over CPU-based QR factorization methods, with a median speedup of over 5x, and achieves up to 200 GFlops as compared to a peak of 79 GFlops for the same algorithm on a multicore CPU.

Our code is available at SuiteSparse.com and as Algorithm 9xx of the Collected Algorithms of the ACM. Consult the user guide in the software bundle for details on how to compile and use the library.

ACKNOWLEDGMENTS
We would like to thank NVIDIA for providing support via their Academic Partner and CUDA Research Center programs, and the National Science Foundation through grant 1115297. We would also like to thank Mohamed Gadou for providing the performance results for MAGMA.

REFERENCES