Wafer Signature Analysis of I_{DDQ} Test Data

Sagar S. Sabade D. M. H. Walker
Department of Computer Science
Texas A&M University
College Station, TX 77843-3112
Phone: (979) 862-4387
Fax: (979) 847-8578
E-mail: {sagars, walker}@cs.tamu.edu

Abstract

Continuous scaling of transistor geometries increases leakage current exponentially. This makes differentiating faulty and fault-free chips extremely difficult. The concept of wafer signature is proposed. A wafer signature is obtained by sorting all I_{DDQ} readings on a wafer for a vector. A break or jump in the wafer signature is considered to indicate defective chips. The use of wafer signatures is evaluated for differentiating faulty and fault-free chips using industrial test data.

Keywords: I_{DDQ} testing, spatial correlation, current signature, wafer signature

1. Introduction

As device geometries are scaled with each technology node [1] leakage current increases exponentially [2]. Elevated background leakage in deep sub-micron (DSM) technologies makes distinction between faulty and fault-free chips difficult. Therefore, the future of I_{DDQ} test is uncertain [3]. Several methods are reported in the literature to solve this problem [4][5][6][7][8][9][10][11][12].

Two methods that have shown promising results are *current signature* [4] and *differential (delta)* I_{DDQ} [5]. Both methods exploit the properties of intra-die vector-to-vector leakage variation to screen defective chips. However, DSM chips show increased inter-die variance [13]. Inter-die I_{DDQ} variation of several orders of magnitude across vectors is observed in practice [14]. This makes distinction between faulty and fault-free I_{DDQ} even more challenging and the conventional single-threshold approach obsolete. In this paper, we borrow ideas from current signature and delta I_{DDQ} methods and extend them to inter-die variation in leakage current to screen defective chips. Wafer level I_{DDQ} data is used to obtain a *wafer signature* and steps (breaks) in this signature are used for screening chips. The method is evaluated using SEMATECH test data[1].

The remainder of the paper is structured as follows. In the next section, we review current signature and delta I_{DDQ} methods and introduce the wafer signature concept. Section 3 discusses the threshold setting issue for wafer signature. Section 4 includes the experimental results, and Section 5 presents the conclusions and future work.

[1] This data comes from the Test thrust at SEMATECH, Project S-121 on Test Methods Evaluation. The conclusions drawn are our own and do not necessarily represent views of SEMATECH or its member companies.

2. Current and Wafer Signatures

The concept of current signature was proposed by Gattiker and Maly [4]. In its simplest form, a current signature is the display of I_{DDQ} readings of a chip sorted in ascending order. Figure 1 shows current signatures for three chips. The basic premise behind current signature is that vector-to-vector variation in the background leakage is small. Thus, a fault-free chip would exhibit a smooth signature (chip 'A' in Figure 1). On the other hand, a chip with a defect would exhibit a jump or step in the signature (chip 'B' in Figure 1). This step indicates the presence of multiple leakage paths that exist due to an *active* (pattern-dependent) defect. In case of a *passive* (pattern-independent) defect, the signature looks similar to that of chip 'C' in Figure 1. In this case, the signature shows that all readings are elevated, although the signature is smooth like that of chip 'A'. An example of a passive defect is a bridge between power supply lines.

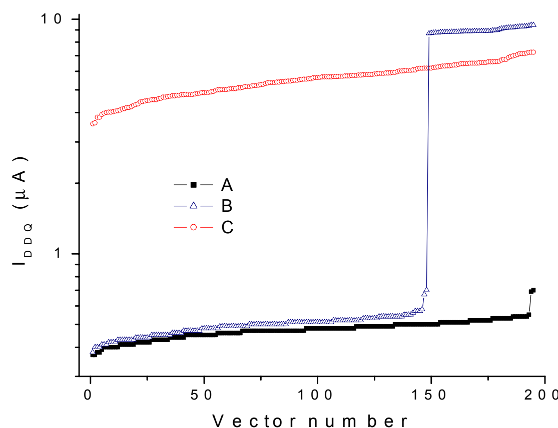

Figure 1. Current signatures for a fault-free (A) chip and chips with active defect (B) and passive defect (C)

Thibeault proposed the idea of differential or delta I_{DDQ} [5]. Delta I_{DDQ} is defined as the difference between I_{DDQ} values for a chip for two consecutive vectors. For a fault-free chip since I_{DDQ} values are similar, the mean delta I_{DDQ} is close to zero and variance is small. In the case of an active defect, deltas are large and the variance is increased. However, in the case of a passive defect, since all I_{DDQ} readings are elevated, average delta and variance are similar to that of a fault-free signature. Both these methods rely on the assumption that intra-die variance is small for a fault-free chip.

The concept of wafer signature is similar to current signature except that a signature is obtained by sorting I_{DDQ} readings for *different die* on a wafer for the *same vector*. Thus, while a current signature depicts intra-die vector-to-vector variation in I_{DDQ}, a wafer signature reveals inter-die variation in I_{DDQ} for a given vector across a wafer. A wafer has as many wafer signatures as the number of vectors with each signature having a number of points equal to the number of die on the wafer.

Both current signature and delta I_{DDQ} require a reasonable number of I_{DDQ} measurements to be successful in discerning fault-free variation. Since I_{DDQ} is a slow-speed test and tester time is expensive, semiconductor manufacturers usually do not gather a lot of I_{DDQ} data. Also, note that for defect detection, current signature and delta I_{DDQ} methods require at least one test pattern that excites the defect and one that does not. This is why even large passive defects may not be screened by these methods. In contrast, wafer signature only requires that at least one vector excite the defect. Thus, a chip having a passive defect will appear in the tail of a wafer signature and will show steps (assuming other chips are fault-free and have low current). Thus, even a single I_{DDQ} reading is enough to detect such chips. In general, the relative impact on quality due to reduction in the number of measurements would be smaller for wafer signature than current signature or delta I_{DDQ}. This is because if a defect is detectable by current signature or delta I_{DDQ} test, it is most likely also detectable by wafer signature.

There are two sources of intra-die variance in a fault-free current signature. The input pattern alters which paths are on/off and therefore I_{DDQ} is a function of input pattern. The second source of variation is due to within-die process variations. This depends on layout geometry, lens aberration, and other processing conditions. The wafer signature eliminates the vector-to-vector variation and depends on the deterministic within-wafer variation. The wafer signature is expected to have larger variance than a current signature.

Figure 2 shows wafer signatures for two wafers for two (identical) vectors. Note that die-to-die correspondence in a wafer signature is lost due to sorting. In other words, chip numbers on the abscissa may not correspond to the same chips. Since the process parameters vary smoothly across a wafer, fault-free chips result in the smooth portion (called the "head") of the wafer signature. Chips having defects appear in the end (called the "tail") of the signature.

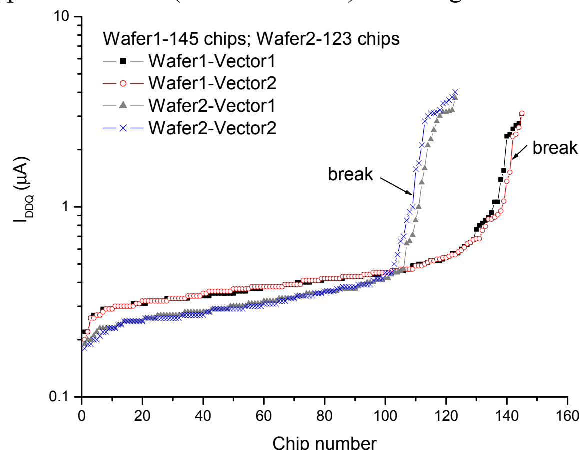

Figure 2. Wafer signatures for two wafers for two vectors

As Figure 2 illustrates, wafer signatures show several "steps" or "breaks". These breaks can occur due to insufficient data from a wafer, process variation-induced intra-die variation across the wafer, and defective chips. The functional yield of a wafer determines the length (number of points) of the signature. A wafer with higher functional yield has more points in a wafer signature and, therefore, a smaller number of breaks (Figure 2). If enough data points (chips) are not available for a wafer (because of poor functional yield or other reasons) or the step size is very small, then the break likely corresponds to the missing data. The breaks also occur in the signature due to defective chips. In SEMATECH data there are approximately 100-200 chips per wafer with more than 70% functional yield. Therefore, it is reasonable to assume that large breaks are due to defects. In the next section, we discuss how to decide whether a certain step size (delta) is small or large, which is essentially a threshold setting issue.

3. Threshold Setting for Wafer Signatures

Breaks in a wafer signature are essentially deltas between I_{DDQ} readings of two chips under the given process conditions. Since process conditions vary smoothly across a wafer, deltas are expected to be small for fault-free chips. The large deltas are assumed to exist due to defective chips. Figure 3 shows the distribution of deltas for all wafer signatures (195 in total) for a wafer. More than 50% of the deltas (17957 out of 32955) are equal to zero.

Use of single threshold

The simplest way to set a pass/fail limit is to select a single threshold value for delta. The threshold could be derived through empirical analysis. However, this method does not account for wafer-to-wafer variation in I_{DDQ} and can result in significant yield loss for some wafers as shown in Figure 4. A 1 µA threshold rejects approximately 3% of the chips from one wafer while 8% of the chips from another. The trend shown in Figure 4 is also observed for

all remaining wafers. The chips with gross defects form a cluster in the tail of a wafer signature and result in a relatively large break. The chips with subtle defects show small breaks throughout a signature. As shown in Figure 4, the plot of number of chips rejected against the threshold shows a plateau (e.g. see region after 1 µA). The chips in this region are most likely to be defective.

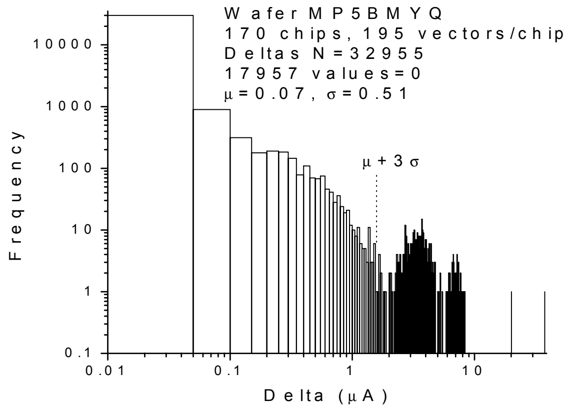

Figure 3. Delta distribution for a wafer for all signatures

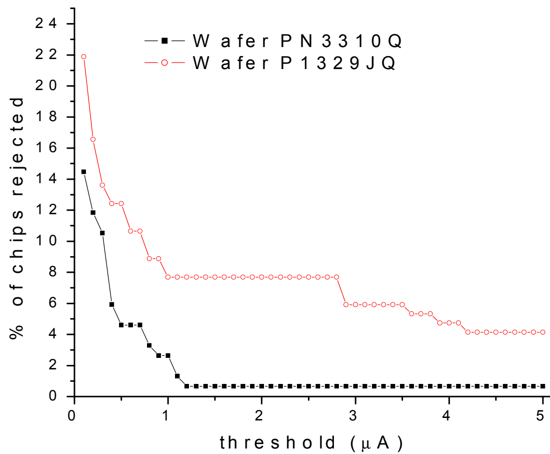

Figure 4. Use of static delta threshold can result in significant yield loss for some wafers

Use of multiple thresholds

It is clear that the delta threshold must be adjusted to account for wafer and lot level variations in I_{DDQ}. Different possibilities exist to achieve this. One way is to set a threshold for each wafer by observing deltas across all signatures. Alternatively, a different threshold can be used for each vector. This threshold should be set for each wafer. Data from several wafers may be combined to decide the nominal step size. Assuming a pass/fail decision is required immediately after wafer probe, wafer-level analysis is used.

As shown in Figure 3, a limit of three standard deviations above the mean may be used for screening chips. Since fault-free and faulty delta values are not known apriori, we try to maximize the number of points in a wafer signature. Therefore, to minimize the number of "dummy" breaks that occur due to missing data, all chips that do not fail functional tests should be used to obtain a wafer signature. Figure 5 illustrates wafer signatures for a wafer with delay failures included and discarded. The heads of the signatures completely overlap and are not shown. Notice that screening chips that fail delay tests can result in several "dummy" breaks in the wafer signature (shown by dotted circle). This can mislead the distinction between faulty and fault-free chips and may result in yield loss.

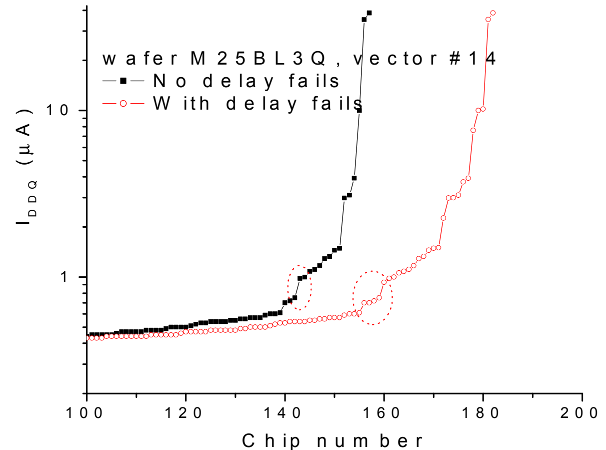

Figure 5. Inclusion of delay failures improves the smoothness of a wafer signature

4. Experimental Results

We used SEMATECH data to evaluate the wafer signature approach to screen defective chips. Even though this data comes from an older technology (0.8 µm drawn, 0.45 µm L_{eff}) [15], the method is equally applicable to state-of-the-art technologies as the physical mechanisms that cause variation in the process remain the same. In the SEMATECH experiment four tests – functional, stuck-at, delay and I_{DDQ} – were conducted at the wafer level. A sample of chips was packaged, subjected to burn-in and all four tests were performed again. I_{DDQ} test used a 5 µA threshold value and a total of 195 readings were measured on each chip.

All chips that failed functional and/or stuck-at test were screened as their I_{DDQ} data is not reliable at least for some vectors. Chips that failed only delay test or delay and I_{DDQ} tests were retained for the reason mentioned in Section 3. Some of these chips could be from a slow wafer region. Gross I_{DDQ} outliers having I_{DDQ} more than 100 µA for any vector were rejected. This limit was selected by observing the I_{DDQ} distribution of the entire population [16]. For each wafer, wafer signatures were obtained for all vectors (195/wafer) and deltas (194/signature) were computed for each signature. All deltas for all signatures for a wafer were combined and a mean+3σ value so obtained was used as the threshold for screening chips. Note that the mean+3σ limit

was computed for deltas but screening was done using the smaller I_{DDQ} value that resulted in the delta exceeding this limit.

For each die, we obtained a current signature by sorting all 195 readings and found the maximum delta (step size). For the delta I_{DDQ} method, we obtained the maximum delta for each die for unsorted data. The delta threshold for current signature and delta I_{DDQ} was varied such that the number of chips accepted by each method that pass all tests at wafer and after burn-in are the same (1053). The current signature threshold was 2.38 μA and that for delta I_{DDQ} was 3.73 μA.

In addition to these three methods, from the distribution of each vector across all chips, the mean+3σ values were obtained and used as thresholds. The distribution of chips according to their test results for each method is shown in Table 1. For each method, the wafer test result and post burn-in results are shown. The chips not burned-in are also shown to illustrate relative yields of each method.

5. Discussion

The disagreement between current signature or delta I_{DDQ} test and wafer signature is noticeable for I_{DDQ}-only failed chips. The chips with passive defects result in small deltas or steps in current signature and are accepted by methods that use intra-die variance for screening. Such chips are rejected by the mean+3 sigma threshold method and, more strongly, by wafer signature. The effect of outliers in the I_{DDQ} distribution affects the properties of the standard distribution. Since this effect is reduced when deltas are obtained the mean+3sigma threshold method accepts more chips than the wafer signature method. Many chips fail only I_{DDQ} test even after burn-in. Due to the stratified nature of the burn-in sample, it is not clear whether the results can be extrapolated to the chips not burned-in with the same accuracy since the actual I_{DDQ} values of these chips are not considered in the analysis.

There are 19 chips that pass all tests at wafer probe and fail at least one voltage test after burn-in. Since none of the methods can catch these chips, these must contain a defect that is not I_{DDQ} testable.

Some chips that fail I_{DDQ} test at wafer probe show reduced I_{DDQ} after burn-in. These so called "healer" chips are unreliable from quality perspective. In a production flow, such healers may not be noticeable as they are rejected at the wafer test itself. These methods show differences in their acceptance and rejection of healers. The differences of various methods in their treatment of healers can be attributed to different thresholds. It might be interesting to distinguish between healers based on the amount of healing. For example, a chip showing pre and post-BI I_{DDQ} variation of (say) less than a 1 μA (for SEMATECH data) can be considered reliable in spite of healing. We did not consider post-BI I_{DDQ} values for this analysis in the present work.

Of particular interest are chips that fail only I_{DDQ} tests before and after burn-in. The differences in number of I_{DDQ}-only failed chips accepted by each method are mostly due to the nature of the defect (active/passive) and due to the smoothness of wafer. The number of chips rejected by wafer signature that do not have BI data is higher than other methods for the same reason.

Table 1. Distribution of test results for different test methods

Method	Accepted Chips		Rejected Chips		Post BI Result
	Wafer Test Result		Wafer Test Result		
	All Pass	I_{DDQ}-only Fail	All Pass	I_{DDQ}-only Fail	
Current Signature	1054	152	2	80	All Pass
	26	198	1	407	I_{DDQ}-only Fail
	19	10	-	11	Voltage Fail
	10119	29	42	37	No Burn-in
Delta I_{DDQ}	1053	88	3	144	All Pass
	26	87	1	518	I_{DDQ}-only Fail
	19	7	-	14	Voltage Fail
	10122	14	39	52	No Burn-in
Wafer Signature	1053	132	3	100	All Pass
	27	149	-	456	I_{DDQ}-only Fail
	19	8	-	13	Voltage Fail
	10068	17	93	49	No Burn-in
Mean + 3 Sigma	1053	157	3	75	All Pass
	27	210	-	395	I_{DDQ}-only Fail
	19	10	-	11	Voltage Fail
	10114	31	47	35	No Burn-in

We computed defect level (DL) and yield loss (YL) for the BI sample as follows.

$$DL = \frac{No.\ of\ \ chips\ \ that\ fail\ \ voltage\ \ test\ after\ BI}{Total\ \ number\ \ of\ chips\ \ accepted} \bullet 100$$

$$YL = \frac{No.\ of\ \ chips\ \ that\ pass\ \ all\ \ tests\ \ at\ \ both\ \ levels}{Total\ \ number\ \ of\ \ chips\ \ rejected} \bullet 100$$

Using the above equations DL and YL values for different methods are tabulated in Table 2. I_{DDQ}-only failed chips were considered fault-free while computing these values.

Table 2. DL and YL for different methods

Method	DL %	YL %
Current Signature	1.99	0.40
Delta I_{DDQ}	2.03	0.44
Wafer Signature	1.94	0.52
Mean+3Sigma	1.96	0.62

It can be seen that no method is a clear winner. The differences in DL/YL are probably too small to draw meaningful conclusions because of the small sample size.

6. Conclusions and Future Work

As device geometries shrink in the future, fault-free leakage current is projected to increase. Distinguishing fault-free and faulty chips from leakage current data is difficult. An alternative approach, called wafer signature, based on the analysis of wafer inter-die I_{DDQ} variance is proposed.

The International Technology Roadmap for Semiconductors (ITRS) indicates that controlling process variations is already a difficult challenge. Especially, intra-die variance will continue to increase making distinction between fault-free and faulty chips using leakage current data more difficult. However, process parameter variation is still expected to be smooth. This is because the underlying physical parameters (e.g. temperature, thickness, etc.) do not change abruptly for fault-free chips. In other words, any abrupt or sudden change in parameter(s) can be attributed to the presence of defects, independent of functional test result. Since no defect-free physical mechanism can explain this behavior, such chips are a high reliability risk. Increasing high reliability requirements with higher levels of integration would necessitate screening such chips in the test flow. The wafer signature approach can provide some insight in identifying such chips in the test flow.

The wafer signature approach relies on the assumption that a reasonably high number of chips have low fault-free I_{DDQ} so that a "step" in the signature is visible. This is a valid assumption for a process with reasonable yield. However, increasing fault-free leakage will affect wafer signatures as the relative size of a step will reduce. Determining fault-free "golden" signatures will require characterization. One possible solution is to exploit defect sensitivities of vectors by comparing different wafer signatures. Thus, one can think of a "difference" signature or area between two overlapping signatures as a metric to screen defective chips.

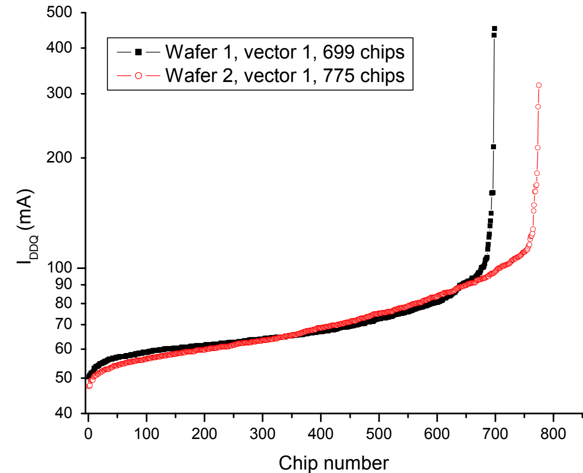

Figure 6. Wafer signatures for the recent technology data

Alternative means for deciding maximum fault-free step size can be considered. This is important for distinguishing between subtle defects and fatally flawed chips. For example, one possible method is to change the threshold depending on the location of the step (number of chips on a wafer clustered before and after the step) based on wafer functional yield information. This can be helpful for differentiating between steps due to missing data and steps due to a defect. Thus for a high-yield process, the threshold may be relaxed in the head of the signature and constrained in the tail of the signature. The threshold may be dynamically adjusted by using wafer-level test information. Different thresholds for different wafer regions may be used to reduce yield loss caused by wafer signature approach.

We believe that wafer signature is simple, straightforward yet neat and scaleable approach for identifying outliers using I_{DDQ} or parametric data. However, like all other variance reduction methods [8, 11, 12], it is constrained by the presence of outliers in the data set. Figure 6 shows the wafer signatures for state-of-the-art technology data. Although leakage current values are much higher than those observed in Figure 2, the wafer-level variation is smooth. Since the fundamental mechanisms that cause fault-free variation do not change, wafer signature approach will be applicable for future technologies.

If wafer test data shows stepper patterns, it must be accounted for while using wafer signature to avoid excessive yield loss. On the other hand, identifying "true" breaks for a very smooth wafer might be difficult. Different methods for threshold setting for wafer signature need to be investigated. Analysis of recent technology data is needed

for better evaluation of this method. How wafer signature approach fares with other approaches when fewer measurements are available is another topic of future investigation.

Acknowledgements

This research was funded in part by Semiconductor Research Corporation under contract 2001-TJ-954 and Texas Advanced Research Program under contract 512-186-2001. The authors would like to thank Dr. Phil Nigh of IBM Corporation for providing the SEMATECH data.

References

[1] International Technology Roadmap for Semiconductors (ITRS), *Semiconductor Industry Association*, 2001, [online] http://public.itrs.net.

[2] J. Figueras and A. Ferré, "Possibilities and Limitations of I_{DDQ} Testing in Submicron CMOS," *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, Part B, Vol. 21, No. 4, Nov. 1998, pp. 352-359.

[3] T. Williams et al., "I_{DDQ} Test: Sensitivity Analysis of Scaling," *IEEE Intl. Test Conference,* Washington D.C., Oct. 1996, pp. 786-792.

[4] A. Gattiker and W. Maly, "Current Signatures: Application," *IEEE Intl. Test Conference,* Washington D.C., Oct. 1997, pp. 156-165.

[5] C. Thibeault, "A Novel Probabilistic Approach for IC Diagnosis Based on Differential Quiescent Current Signatures," *IEEE VLSI Test Symposium*, Monterey, CA, Apr. 1997, pp. 80-85.

[6] P. Maxwell et al., "Current Ratios: A Self-scaling Technique for Production I_{DDQ} Testing," *IEEE Intl. Test Conference,* Atlantic City, NJ, Oct. 1999, pp. 738-746.

[7] S. Jandhyala et al., "Clustering Based Techniques for I_{DDQ} Testing," *IEEE Intl. Test Conference,* Atlantic City, NJ, Oct. 1999, pp. 730-737.

[8] W. R. Daasch et al. "Variance Reduction Using Wafer Patterns in I_{DDQ} Data," *IEEE Intl. Test Conference,* Atlantic City, NJ, Oct. 2000, pp. 189-198.

[9] C. Thibeault, "An Histogram Based Procedure for Current Testing of Active Defects," *IEEE Intl. Test Conference*, Atlantic City, NJ, Oct. 1999, pp. 714-723.

[10] A. Keshavarzi et al., "Multiple-Parameter CMOS IC Testing with Increased Sensitivity for I_{DDQ}," *IEEE Intl. Test Conference,* Atlantic City, NJ, Oct. 2000, pp. 1051-1059.

[11] S. Sabade and D. M. H. Walker, "Improved Wafer-level Spatial Analysis for I_{DDQ} Limit Setting," *IEEE Intl. Test Conference,* Baltimore, MD, Oct. 2001, pp. 82-91.

[12] S. Sabade and D. M. H. Walker, "Neighbor Current Ratio (NCR): A New Metric for I_{DDQ} Data Analysis," *IEEE International Symposium on Defect and Fault Tolerant Systems*, Vancouver, Canada, Nov. 2002, pp. 381-389.

[13] C. Hawkins and J. Soden, "Deep Submicron CMOS Current IC Testing: Is There a Future?," *IEEE Design and Test of Computers*, Vol. 16, No. 4, Oct.-Dec. 1999, pp. 14-15.

[14] J. Diez and J. Lopez, "Influence of Manufacturing Variations in I_{DDQ} Measurements: A New Test Criterion," *Design Automation Conference*, Los Angeles, CA, June 2000, pp. 645-649.

[15] P. Nigh et al., "So What is an Optimal Test Mix?: A Discussion of the SEMATECH Methods Experiment," *IEEE Intl. Test Conference*, Washington, DC, Oct. 1997, pp. 1037-1038.

[16] S. Sabade and D. M. H. Walker, "Wafer-level Spatial and Flush Delay Correlation Analysis for I_{DDQ} Estimation," *IEEE Intl. Workshop on Defect Based Testing*, Monterey, CA, Apr. 2002, pp. 47-52.