CodSim – A Combined Delay Fault Simulator

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Abstract

Delay faults are an increasingly important test challenge. Traditional delay fault models are incomplete in that they only model a subset of delay defect behaviors. To solve this problem a combined delay fault (CDF) model has been developed, which models delay faults caused by the combination of spot defects, parametric process variation, and capacitive coupling. The spot defects are modeled as both resistive opens and shorts. The CDF model has been implemented in the CodSim delay fault simulator which gives more realistic delay fault coverage. The fault coverage of traditional test sets has been evaluated on the ISCAS85 circuits.

1. Introduction

The 2002 International Technology Roadmap for Semiconductors (ITRS) [1] projects at-speed testing as an increasingly difficult problem. Rising clock frequencies and the increasing influence of interconnect on circuit delays are making traditional functional and delay test approaches inadequate.

As shown in Figure 1, spot defects and parametric process variation can cause functional failures, delay faults, or reliability hazards. A *local delay fault* is a local delay increase caused by a spot defect, such as a resistive open or short. The gate or transition fault model targets these faults. Global delay faults are slow paths due to process parameter variation such as transistor gate length variation. The path delay fault model targets these faults. *Combined delay faults* (CDF) are delay faults caused by a combination of spot defect and process variation. By considering the entire range of spot defect parameters and process variation, the CDF model encompasses both local and global delay faults.

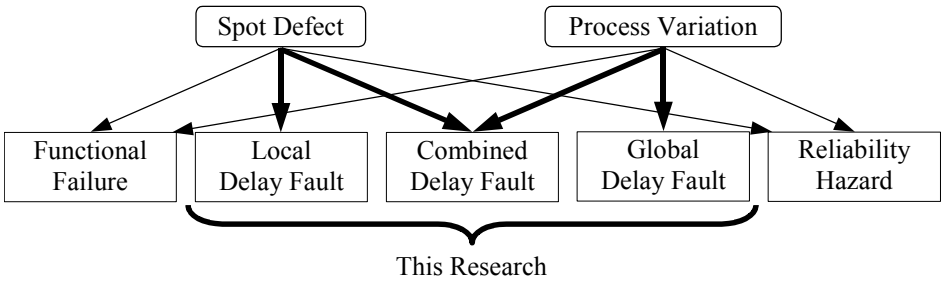

Figure 1. Fault types addressed in this work.

The traditional delay fault models do not completely describe all realistic fault behaviors, and so result in incomplete fault coverage and poor diagnostic resolution. In particular they do not account for pattern-sensitive delay due to signal coupling and resistive shorts [2]. Capacitive coupling causes significant variation in path delays [3][4][5]. The behavior is even more complicated when resistive opens or shorts are combined with capacitive coupling [6][7].

In this research we propose to use a physically realistic yet economical combined delay fault model to simultaneously account for delay faults due to resistive opens and shorts, and parametric process variation, in the presence of capacitive coupling. At this time we do not consider delays due to inductive coupling, power supply noise [8] or substrate noise.

We have implemented the CDF model in the *CodSim* (**Co**mbined **D**elay Fault **Sim**ulator) delay fault simulator and used it to evaluate the CDF coverage of existing test sets on the ISCAS85 benchmark circuits. The CDF coverage has been compared with the fault coverage using traditional fault models, such as the transition fault model. As was the case for Boolean test of resistive bridges [9], results show that the loss in coverage is primarily due to faults with low detection probability [9][10].

The remainder of the paper is organized as follows. Section 2 describes the combined delay fault model and its coverage metric. Section 3 describes the fault simulation algorithm and Section 4 includes experimental results. Section 5 concludes with directions for future research.

2. Fault Model and Coverage Metric

In the combined delay fault model it is assumed that there is only one spot defect in the circuit, and the circuit is also subject to process variation and capacitive coupling. In this model, fault detection is probabilistic instead of deterministic. For example, suppose there are two paths, P_1 and P_2, through an open fault site. Figure 2 shows the delays of the two paths, and the delays have a distribution due to process variation. t_{max} is the maximum specified delay of the circuit. Δ is the extra delay at the fault site. A transition test [11] would test either P_1 or P_2 and 100% transition fault coverage is achieved. This is valid only if Δ is large. A gate delay test [12] would test P_1 because P_1 has a larger nominal delay. Testing P_1 can detect a smaller extra delay than testing P_2. However, in reality testing P_1 only does not guarantee 100% detection, because when the extra delay is between Δ_1 and Δ_2, testing P_1 may not detect the fault while testing P_2 may detect it, assuming the delays of the two paths are not perfectly correlated. A path delay fault test [13] tests both paths, and assumes the path delay is pattern independent. However, if the worst-case capacitive coupling along the path can be sensitized (the delay distribution of P_1 becomes P'_1), a smaller extra delay Δ' would escape the path delay test.

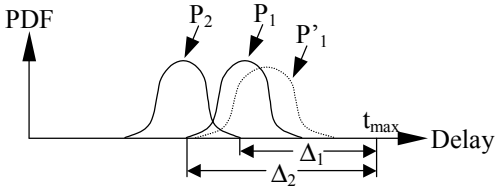

Figure 2. Probabilistic fault detection.

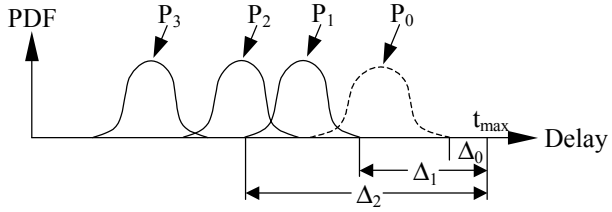

Figure 3. Fault coverage computation.

Thus no traditional delay fault test is able to guarantee detection of realistic faults. To achieve 100% fault coverage under the CDF model, all the paths which can be the longest path through the fault site (in this example, both P_1 or P_2) must be tested, with the worst-case capacitive coupling sensitized. Moreover, because of process variation, the coupling sensitization is also probabilistic. Therefore, all the test patterns which sensitize the worst-case coupling under every process parameter combination must be applied.

A fault coverage metric for the CDF model is developed to evaluate the quality of existing test sets. In this research the notion of detection probability (DP) [9][10] for a single fault site is used. Suppose a test set t has been applied to the circuit. For fault site i, and the local extra delay Δ caused by the spot defect [14], the DP is [15]:

$$\mathbf{DP}_{i,\Delta}(t) = \mathbf{P}(t \text{ detects delay fault} \mid \text{chip has a delay fault}) \quad (1)$$

We define "t detects delay fault" as "at least one path tested by t through fault site i is slow", and for simplicity, we regard "chip has a delay fault" when $\Delta > \Delta_0$ in Figure 3, where Δ_0 is the smallest detectable extra delay. This delay can only be detected by sensitizing the longest path (P_0 in Figure 3) through the fault site and this path is assumed to be under the worst process corner. Here "longest" means "maximum delay with the worst-case coupling sensitized". Thus the definition can also be written as:

$$\begin{cases} \mathbf{DP}_{i,\Delta}(t) = \mathbf{P}(\text{at least one tested path through } i \text{ is slow}) \\ \Delta > \Delta_0 \end{cases} \quad (2)$$

In Figure 3, suppose paths P_1, P_2 and P_3 are tested by t, and P_0 is not tested. When $\Delta_0<\Delta<\Delta_1$, $DP_{i,\Delta}(t)$ is 0; when $\Delta>\Delta_2$, $DP_{i,\Delta}(t)$ is 100%, because the tested path P_1 is definitely slow; when $\Delta_1<\Delta<\Delta_2$, $DP_{i,\Delta}(t)$ increases from 0 to 100% as Δ increases.

The fault coverage metric tells us that there are two ways to get a higher-DP test:

1. Increase the delay of the longest tested path by either testing a longer path or sensitizing the worst-case coupling, to reduce the 0-DP area between Δ_0 and Δ_1.

2. Test more paths whose delays are close to the longest tested path (such as P_2 in Figure 3) or increase the delay of such paths to increase the DP between Δ_1 and Δ_2. Testing a short path (such as P_3) does not increase the DP because whenever it is slow, the longest tested path P_1 must be slow too.

The above analysis is for a given local extra delay Δ. For fault site i with an arbitrary Δ, the DP for site i is computed as:

$$\mathrm{DP}_i(t) = \int_{\Delta>\Delta_{0,i}} \mathrm{DP}_{i,\Delta}(t) \cdot \mathrm{p}_i(\Delta)\mathrm{d}\Delta \quad (3)$$

where $p_i(\Delta)$ is the PDF of Δ at fault site i, and can be computed using the PDF of the open or bridge resistance [14]. The DP computation for resistive shorts is more complicated than that for resistive opens, because both shorted lines can be slowed down. The extra delays on both lines must be computed.

The overall fault coverage for test set t (for both open and bridge faults) is:

$$\mathrm{FC}(t) = \sum_i \mathrm{DP}_i(t) \cdot w_i \times 100\% \quad (4)$$

where w_i is the weight for fault site i ($\sum_i w_i = 1$). In our experiments, for simplicity, w_i is set to $1/N$, where N is the total number of open or bridge fault sites, assuming all sites are equally likely.

3. Simulation Algorithm

The goal of the combined delay fault simulation is to compute the detection probability for each fault site, for test set t. If the DP is high enough, the fault site can be dropped so that ATPG is not required for that site. The DP's for all the fault sites are then used to compute the overall fault coverage, so that the quality of the test set is evaluated.

Figure 4 shows the three phases in the CDF simulation algorithm. In the first phase, spot-defect-free timing simulation is performed for each vector pair. After the simulation, the initial and final logic values and the nominal transition time of the last event for each line are known. Figure 5 shows an example. The italic numbers next to the transition symbols indicate the transition time, assuming the unit gate delay model is used. S1 or S0 indicates a stable logic value 1 or 0 on the line.

1. For each test vector pair, run spot-defect-free timing simulation and identify the robust/non-robust propagation paths from each line to primary outputs.
2. Check the validation of the non-robustly sensitized paths through a line, by introducing a spot defect at that line and running fault simulation.
3. Run fault simulation considering coupling for the selected long paths for each fault site.

Figure 4. CDF simulation algorithm.

Then the robust/non-robust propagation paths [13][16] from each line to primary outputs are identified. A line's robust propagation paths can be computed using its immediate fanout lines' robust propagation paths. In Figure 5, suppose line d has a robust propagation path P_1 with length 6, and line e has path P_2 with length 7. The robust propagation paths for line b are computed by checking the final logic values on the side inputs of gate G_1 and G_2. Then two paths are identified: b-P_1 with length 7 and b-P_2 with length 8. Because the propagation paths are robust, the slow signal is able to propagate through these paths independent of the delays on the side inputs to the paths. Therefore the extra delay Δ on a line must be detected if $t_{trans} + \Delta + l_{prop} > t_{max}$, where t_{trans} and l_{prop} are the transition time and propagation path length associated with that line, respectively. In the simulation, since t_{trans} and l_{prop} are statistical values (with PDFs), the computed Δ is a statistical value too. For resistive shorts, the sensitization condition, i.e. the opposite logic value on the other shorted line, must be checked.

The non-robust propagation paths can be identified in a similar way. The difference is that if there is no transition on a line, the non-robust propagation paths from that line must also be computed. Line g in Figure 6 is an example. The reason is that a spot defect on line d may generate a glitch on g, and the computation of the non-robust propagation paths from d uses g's propagation paths. The complexity of phase 1 is $O(V \cdot C)$, where V is the number of vectors and C is the circuit size (number of lines in the circuit).

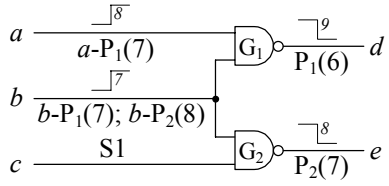

Figure 5. Robust propagation path indentification.

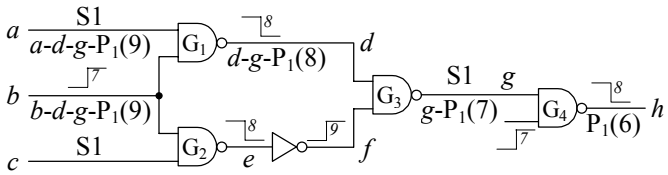

Figure 6. Non-robust propagation path identification.

A problem with the non-robust propagation paths is that the fault detection through these paths is dependent on the delays on the side inputs to the path. In Figure 6, an extra delay on line b does not affect the transition time on line h, even though line b has a non-robust propagation path. Therefore, the validation of these paths must be checked (phase 2). After phase 1, each line has a few non-robust propagation paths. The validation check can be performed by introducing an extra delay Δ on the line, where $\Delta = t_{max} - t_{trans} - l_{prop}$, and running fault simulation for the vector which sensitizes this path, to check if the slow signal can be detected at any primary output. This procedure starts from the smallest Δ. If a small Δ can be detected through a non-robust propagation path, the validation check for the paths which can only detect large Δ is not necessary, because testing those paths, such as P_3 in Figure 3, does not increase the fault coverage. Experiments show that normally only a few paths must be checked for each line.

It is possible that some functional sensitizable paths [17] are missed. However, because these paths always appear in pairs and the delay is determined by the shorter one, in most cases they

do not contribute to the fault coverage. Thus these paths are not checked unless there is no long robust or non-robust propagation path through the fault site.

In phase 3, the extra delay due to coupling is computed. Similar to phase 2, phase 3 introduces an extra delay Δ at the fault site, where Δ can cause one propagation path (either robust or validated non-robust) to be slow, and runs the fault simulation considering coupling for the vector sensitizing the path. The reason why Δ should be introduced is because the coupling alignment is dependent on Δ. Handling capacitive coupling is a classic "chicken and egg" problem, because the victim's transition time depends on the aggressor's timing window, which could depend on the victim's output [18]. We solve this problem by iterative simulation, which is similar to the algorithm used in [18]. Similarly, phase 3 is only performed for the long paths.

4. Simulation Results

A combined delay fault simulator *CodSim* was developed in Visual C++ and run on Windows 2000 with a 450 MHz Pentium III processor. In the experiments, random coupling net pairs with realistic coupling capacitance values are included. Buffer-to-buffer delays are assumed to have a normal distribution with 3σ = 15% of the nominal delay. The smallest detectable open resistance is computed using the longest sensitizable path through the fault site [19], and it is assumed that the path delay would increase by 3% if the worst-case coupling is sensitized [4]. For shorts, different cases for the two shorted lines are analyzed and the largest detectable resistance is computed.

Table I shows the open fault coverage for the ISCAS85 circuits, simulated using 10 000 random vectors and transition tests, which are generated by Mentor Graphics FastScan™ using a backtrack limit of 200. Circuit c2670 is not included due to a circuit layout extraction problem. In this work, it is assumed that 80% of the open faults have infinite resistance, while 20% are resistive, with log(R) uniformly distributed, where R is the open resistance [20].

Table I. Fault simulation results for resistive opens.

Circuit	Open Sites	10 000 Random Vectors			Transition Test			
		Tran. FC (%)	CDF Cov. (%)	Sim. Time (s)	# of Vec.	Tran. FC (%)	CDF Cov. (%)	Sim. Time (s)
c432	432	99.2	99.1/97.6	1.9	182	99.4	98.8/96.6	0.1
c499	499	99.1	98.9/94.0	3.0	184	99.4	98.6/93.6	0.1
c880	880	100	99.3/96.0	6.2	182	100	98.8/96.2	0.1
c1355	1 355	99.5	98.6/94.0	7.5	550	99.8	96.4/93.4	0.6
c1908	1 908	95.8	94.9/92.4	12.1	500	99.7	98.4/96.3	1.2
c3540	3 540	91.8	91.1/88.6	22.1	608	96.3	94.9/93.0	1.8
c5315	5 315	94.9	94.7/92.7	49.1	402	99.5	99.0/98.4	2.7
c6288	6 288	99.1	96.1/93.6	44.6	190	99.2	96.2/94.2	1.1
c7552	7 552	92.1	91.9/89.7	70.7	696	98.4	98.1/96.4	5.8

Column 2 shows the number of open fault sites, assuming an open may happen on the inputs and output of any gate in a circuit. Columns 3 and 7 show the fault coverage using the transition fault model, in which the local delays are assumed to be large. Recent research [21] shows that real delay fault coverage is slightly higher, since most delay faults are due to resistive opens that affect both transitions. The fault coverage using the CDF model is listed in columns 4 and 8, assuming a full-speed/half-speed test is applied. For the long random test set, the fault coverage using a full-speed test is close to its transition fault coverage (<1% difference), because a fault site has high probability to have many long paths tested. The CDF coverage loss for the random test set is primarily due to the faults which have zero detection probability, i.e.

no path through the fault is tested. The transition test ensures that at least one path through each non-redundant fault site is tested, therefore the CDF coverage loss is primarily due to the fact that not enough long paths through the fault site are tested. Circuit c6288 is an interesting case because the CDF coverage is not close to the transition fault coverage. The reason is that for this circuit, it is very easy to sensitize one path through each gate/line but it is very hard to sensitize a long path through a gate/line. The CDF coverage for testing the 10 longest non-robustly testable paths through each gate (10-LPEG test) [19] is 99.9%+, if the redundant open faults are removed. The number of vectors is listed in Table III.

Table II shows the resistive bridge fault coverage for the ISCAS85 circuits. Random non-feedback shorts are used. The number of shorts is approximately twice the number of lines in the circuits. Shorts between lines feeding the same gate are not included. Shorts between the signal lines and power/ground grid are not considered because they are more likely to behave as stuck-at or transition faults. The bridge resistance is assumed to be uniformly distributed between 0 Ω and 40 kΩ [22].

Table II. Fault simulation results for resistive shorts.

Circuit	Bridge Sites	10 000 Random Vectors			Transition Test			
		0 Ω FC (%)	CDF Cov. (%)	Sim. Time (s)	# of Vec.	0 Ω FC (%)	CDF Cov. (%)	Sim. Time (s)
c432	821	99.4	88.1/84.4	1.4	182	93.3	81.4/81.0	0.1
c499	1 102	99.9	93.5/89.4	2.2	184	96.5	86.7/81.3	0.1
c880	1 421	99.6	90.9/86.2	2.4	182	95.7	85.3/83.5	0.1
c1355	2 488	99.5	88.6/84.2	7.0	550	97.3	84.8/81.6	0.3
c1908	4 007	98.3	92.0/91.9	5.1	500	96.8	88.4/88.1	0.4
c3540	8 919	96.8	87.0/86.7	17.9	608	93.6	80.3/80.0	1.4
c5315	12 168	98.0	94.3/94.0	18.6	402	97.1	89.4/89.1	1.3
c6288	14 170	99.2	91.6/91.4	22.5	190	92.9	78.8/78.6	1.0
c7552	12 156	94.2	87.2/86.6	25.7	696	95.8	82.8/81.9	2.8

Columns 3 and 7 show the fault coverage using the 0 Ω bridge fault model. For both random and transition test sets, there is a large CDF coverage loss, and it can be seen that the CDF coverage does not increase much if the test speed is increased. Figures 7a and 7b explain the phenomenon. The delay caused by most resistive shorts can be plotted as shown in Figure 7 [14]. For most shorts, the slack of the longest sensitizable path through either shorted line is not very tight (Figure 7a), therefore the coverage loss, which is the range between the two dotted vertical lines, is small, even if a half-speed test is applied. However, for some shorts with one shorted line on a critical path, a large coverage loss occurs if the longest sensitizable path through that line is not tested (Figure 7b).

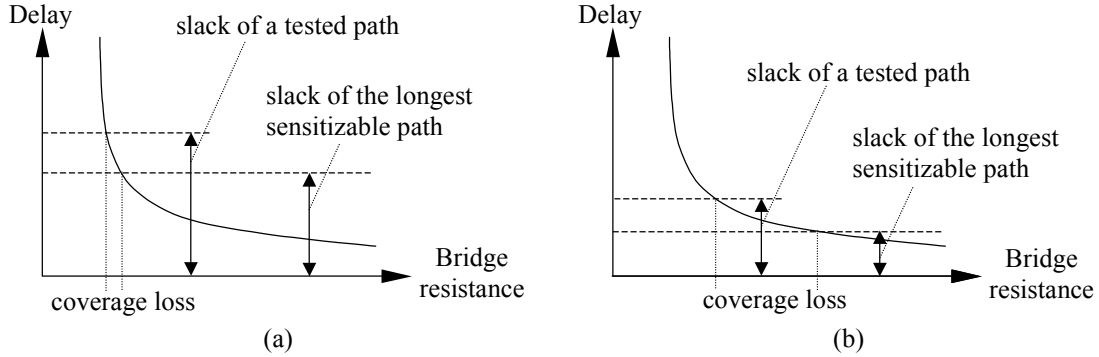

Figure 7. Delay vs. Bridge resistance.

It can also be seen from column 3 in Table II that the long random test sets do not result in many 0-DP bridge faults though they cause many 0-DP open faults. This is because a bridge fault can be detected by either shorted line in most cases. However, since large bridge resistance can be detected only through the line with weaker drivers, high 0 Ω bridge fault coverage does not necessarily indicate high CDF coverage for resistive shorts. Transition tests have low CDF coverage because they do not have high probability to set the opposite logic value on the other shorted line when a transition occurs on the line with weaker drivers.

Table III shows the results for resistive shorts using the 10-LPEG tests generated in [19]. Column 2 shows the number of vectors. The vectors are not compacted so one vector pair targets one path. Column 3 shows the fault coverage using full-speed tests. It can be seen that by testing the 10 longest paths through each gate, higher CDF coverage for resistive shorts is achieved. Though the tests do not aim at the bridge faults, by testing the shorted line with weaker drivers at least 10 times, it is likely that at least one test vector sets the opposite logic value on the other shorted line. And since the fault is propagated through many long paths, the coverage loss is small, and primarily due to the fact that the worst-case coupling for those paths is not sensitized.

Table III. Results for resistive shorts using 10-LPEG tests.

Circuit	# of Vectors	Full-speed Test FC (%)	Sim. Time (s)
c432	840	97.4	0.2
c499	3 064	98.4	0.8
c880	2 046	98.5	0.6
c1355	3 922	97.6	2.9
c1908	3 108	99.5	2.0
c3540	7 784	99.7	13.6
c5315	8 720	99.6	18.2
c6288	14 448	99.1	35.7
c7552	11 976	98.4	30.2

5. Conclusions and Future Work

In this work we have described a physically realistic combined delay fault model incorporating the delay effects of spot defects, parametric process variation and capacitive coupling. The CDF model uses the accurate delay models we have developed [14]. We have implemented the CDF model and a fault coverage metric in the *CodSim* delay fault simulator.

Experiments show that full-speed tests are able to detect most open faults, while the bridge fault coverage is not high, using some traditional test sets. The reason is because for some bridge faults, large coverage loss occurs if the longest true paths through them are not tested. Due to this reason, testing the K longest paths through each gate results in high CDF coverage for resistive shorts.

The future direction of our work is to use the *CodSim* simulator in the *CodGen* delay test ATPG framework [19]. So far *CodGen* only generates the K longest paths through each gate. In order to maximize the CDF coverage for resistive shorts, *CodGen* should target the bridge faults and maximize the delay due to coupling. On the other hand, it must incorporate spatial process correlation to reduce the test size without coverage loss.

Acknowledgements

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