A Practical Built-In Current Sensor for I_{DDQ} Testing

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Abstract

This paper describes a new built-in current sensor (BICS) design, comprised of a MAGFET current sensor, stochastic sensor, self-calibration tool, counter, and scan chain. By indirectly measuring the current, the sensor avoids the unacceptable drawbacks of past BICS designs. Test chips fabricated in 180 nm and 250 nm technology demonstrate that the sensor can be used for I_{DDQ} testing of large, high-performance, deep sub-micron circuits. This sensor should extend practical I_{DDQ} testing to the 35 nm technology generation.

1. Introduction

Quiescent current (I_{DDQ}) testing has shown very good coverage of physical defects such as gate oxide shorts, floating gates, and bridging faults which are not very well modeled by classical fault models, or undetectable by conventional logic tests. The demand for high quality and cost effectiveness necessitates a wide use of I_{DDQ} testing as a supplementary test to voltage tests. When combined with other test techniques, it has the potential for eliminating the need for burn-in test [1][2][3]. However MOSFET leakage currents are rising rapidly with each technology node, narrowing the difference between the I_{DDQ} levels of a faulty and fault-free circuit [4].

In recent work [5] we used data from the 1999 International Technology Roadmap for Semiconductors (ITRS99) [6] to determine the requirements for I_{DDQ} testing to remain practical and useful in future technology nodes. These requirements are summarized as follows:

- Good fault coverage through multiple technology nodes. Prior work has shown that most defective chips with anomalous I_{DDQ} have I_{DDQ} levels 5-100 μA or more above their nominal values [2][3][7][8]. As circuit performance increases, many of today's I_{DDQ}-only failures will cause delay faults [9]. To remain competitive with more effective delay testing, an I_{DDQ} test must screen out faults that cause elevated I_{DDQ}, but not a delay fault. The analysis in [5] showed that to be able to detect faults in the 35 nm node that may not cause a delay fault, but form a reliability hazard, 2 μA changes in IDDQ must be detectable. Given the normal variation in I_{DDQ} [10], this requires background I_{DDQ} levels to be less than 10 μA in order for the maximum random variation to equal the defect-generated current. This limit can be relaxed by as much as 30-40 times through the use of resolution enhancement schemes such as current signatures [11], differential IDDQ [12][13], delta IDDQ testing [14], current ratios [15][16], and current clustering [17][18].
- Circuit performance loss < 1% and no significant increase in power supply noise due to any on-chip I_{DDQ} design-for-test (DFT) circuitry.
- Chip area overhead < 1% for DFT circuitry.
- No special semiconductor processing steps.
- Test time of about 1 ms/vector. This implies that if large numbers of built-in current sensors (BICSs) are used on the chip, they must be able to operate in parallel, or else be extremely fast. This also implies that such BICSs must contain an analog-to-digital converter (ADC) since it is not feasible to quickly read out many analog signals.
- Ability to measure the current level, not just a pass/fail signal. Current levels are needed for resolution enhancement techniques.
- For a built-in current sensor (BICS), the ability to measure current direction. In a mesh-type supply network, the current flow along a supply branch can be in either direction, depending on interconnect process variation or defects.
- Scan chain control of any DFT circuitry.
- Usable at wafer and package test.
- Ability to isolate faults for diagnosis.
- DFT circuitry must have reasonable power dissipation when in use, and low or no dissipation when inactive.

Our prior analysis [5] showed that resolution enhancement techniques alone are not sufficient to apply I_{DDQ} testing in future technology nodes. The only feasible solution is to combine such techniques with BICSs. Our analysis showed that the number of BICSs without resolution enhancement would rise from 2 in the 180 nm technology node to more than 2000 in the 35 nm node for low-power chips, and from nearly 6000 to more than 10 million for high-performance chips. The latter is too many to meet the chip area overhead requirement, but in combination with resolution enhancement it should be feasible.

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The goal of this research is to develop a BICS design that meets the above requirements. To summarize, the BICS requirements are:

- < 2 μA resolution
- < 1000 transistors in size
- < 1 ms/vector test time
- Does not cause performance degradation
- Measures current level and direction
- Control and digital readout via scan chain
- Parallel operation
- Self-calibration
- Low power dissipation in use, none when idle

The following sections describe the BICS and our experimental results. Section 2 describes the sensor design. Section 3 describes its operation during I_{DDQ} test. Section 4 describes experimental results, and Section 5 concludes.

2. BICS Design

To meet the I_{DDQ} testing requirements described in Section 1, we propose a new I_{DDQ} sensor system shown in Fig. 1. The system is comprised of a MAGFET current sensor, stochastic sensor, calibration tool, and counter/scan chain [19].

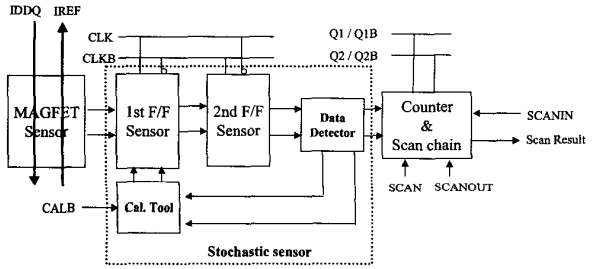

Fig. 1 Proposed MAGFET I_{DDQ} Sensor

The current sensor is implemented using a split-drain MAGFET that indirectly measures the I_{DDQ}. The I_{DDQ} in a supply line generates a magnetic field, which is sensed by the MAGFET. The MAGFET uses the Hall effect generated by the Lorentz force on moving carriers in the MOS transistor channel. The moving carriers deflected by the Lorentz force generate a current difference between the two drain terminals, with a linear relationship between the current difference and the magnetic field, and thus I_{DDQ}. This non-invasive method avoids any performance penalty during normal circuit operation. It can be used to sense the current on any branch of the supply network, and so can be used to monitor mesh-type supply networks. It will also generate a positive or negative signal depending on the direction of current flow. A split-drain MAGFET sensor has high sensitivity even with a small bias current and so low power dissipation. It can be shut off when not in use.

The stochastic sensor consists of two flip-flops, a data detector, and a calibration tool. The stochastic sensor amplifies the small MAGFET signal and generates a bit stream of "0" and "1" values to the counter which accumulates them. A self-calibration tool nulls out any circuit imbalance when no input signal is present. The flip-flops achieve high sensitivity by operating in the metastable region [20]. They compare the input signal to the random noise to determine which way to flip. The data detector converts this flip to a counter clock pulse. The counter value is the digital representation of the signal, so the stochastic sensor plus counter form an ADC. The counter value can then be scanned out. The stochastic method has two advantages: an ADC can be implemented in a small area using digital components, and it can measure a signal much smaller than the random noise.

In the following sections we describe the BICS components in detail. Our general strategy to achieve high resolution is to first design the MAGFET for high signal-to-noise ratio (SNR), and then to design the stochastic sensor to achieve high resolution.

A. MAGFET Design

In order to avoid performance loss during normal circuit operation, the current sensor must be noninvasive. Two means of doing this are to measure the voltage drop across the parasitic resistance of a segment of the supply line, and measure the magnetic field generated by the current flow. Voltage drop sensing has been used successfully in analog circuits [21], but is not suitable for digital circuits due to the large peak to minimum supply current range. Sensing the magnetic field has been previously attempted [22][23], but the prior work did not meet many of the requirements outlined in Section 1.

As an orthogonal Hall sensor, the MAGFET has been considered one of the best candidates for intelligent micro-systems because of its full compatibility with CMOS processing and its good linearity, which is essential for sensing small magnetic fields [24]. The high current density of the thin inversion layer formed under the gate is effective in producing a larger Hall voltage, even though the carrier mobility is lower than bulk silicon [25]. Therefore we chose the MAGFET as our magnetic field sensing device.

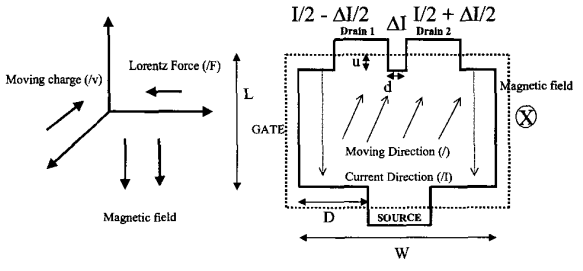

Fig. 2 Principle of split-drain MAGFET sensor

Fig. 2 shows the structure of the current-crowding split-drain MAGFET and the effect of magnetic field on carriers in the inversion layer. When the MAGFET is exposed to a magnetic field, *B*, perpendicular to the device surface, it results in a current imbalance *ΔI=I1-I2* between

the two drains that is proportional to the vertical component of the magnetic field.

In MAGFET design, our primary goals are to achieve high current sensitivity, high voltage gain and high SNR in as small of an area as possible. By using a MAGFET with narrowed source and drain contact area, we crowd the current flow into the center of the channel. This increases the fraction of the current that has a chance to flow out one drain or the other, improving sensitivity. Crowding is further increased by only placing drain contacts near the notch between the two drains. Crowding increases the current density in the central area of the channel by 3 to 4 times. The channel resistance increases by 1.4 times. High channel resistance for given MAGFET dimensions achieves higher output voltage gain (discussed below) and lower bias current, while maintaining a low noise level.

The MAGFET sensitivity ($\Delta I/B$) is a function of the MOSFET device geometry, including drain gap (d), gate poly overlap (u), width/length ratio (W/L), and bias condition [26]. Through circuit simulations [27] we determined that a W/L of 0.7 was the optimum to achieve high sensitivity and high SNR. The most challenging aspect of the simulations was developing an adequate noise model. The optimum bias voltage is $V_{DD}/2$ to ensure that the MAGFET is in saturation when used in the cross-coupled circuit described in the next section.

B. Cross-coupled MAGFET

In addition to maximizing the MAGFET sensitivity, we organized two P-type and N-type MAGFETs in a cross-coupled fashion (Fig. 3) to yield a higher current sensitivity and higher voltage gain. The P-type and N-type MAGFETs are oriented and their drains connected so that for a given magnetic field, the drain of one type (P) MAGFET with increased current is connected to the drain of the other type (N) MAGFET with decreased current, and vice versa. So the current difference between the two outputs are added to generate $2\Delta I$. The common bias current I flows from the P-type to the N-type MAGFET.

Within the cross-coupled circuit, each MAGFET acts as an active load to the other. Each MAGFET is biased to be in saturation ($V_{DD}/2$) so that its sensitivity will be relatively constant over a reasonable output voltage range, and so that the load resistance will be high to provide high voltage sensitivity [25]. The MAGFET bias voltage is provided by an inverter with its input tied to its output. The inverter devices are matched to the MAGFETs so that the bias is maintained with process variation.

The characteristic curve of the cross-coupled MAGFET is shown in Fig. 3. For channel output impedance R_{CH}, the cross-coupled MAGFETs output voltage difference is $\Delta V = 2R_{CH}\Delta I$. To achieve high voltage gain, we use long-channel MAGFETs. In order to reduce 1/f noise, we also use a wide channel. The MAGFETs are sized to provide approximately the same conductance for the P-type and N-type devices. For an N-type MAGFET W/L of 140 μm/200 μm, the circuit provides a gain of 100–120 dB, and a differential output voltage centered at $V_{DD}/2$. The linear output range is 10-20 mV around the operating point. Since we expect output voltages of 0.33 μV to 1 mV, this is more than sufficient to accommodate the I_{DDQ} range of interest.

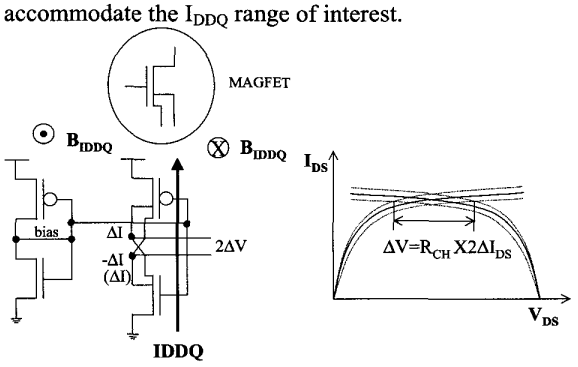

Fig. 3 Cross-coupled MAGFET sensor

C. MAGFET Noise Control

In addition to increasing gain, we must also ensure that the MAGFET has a high SNR. This is especially true since the noise will be comparable to or larger than the signal. We apply two approaches to increase the SNR. One is to cancel out external magnetic field noise from nearby electrical equipment (e.g. the tester, other on-chip circuitry), and the Earth's magnetic field (B_{EARTH}). The second approach is to reduce the internal noise of the MAGFETs. B_{EARTH} is 60-100 μT, which is much higher than the field generated by the I_{DDQ} (B_{IDDQ}) A 2 μA current in a wire 10 μm from the MAGFET will generate a field of 40 nT. So the effect of B_{EARTH} must be reduced by a factor of more than 1000. To cancel out B_{EARTH}, we use two pairs of cross-coupled MAGFETs hooked up in parallel, placed on either side of the supply line, with connections swapped so that they produce opposing signals due to the same magnetic field [23]. The circuit diagram is shown in Fig. 4, and a possible layout is shown in Fig. 5. Since B_{IDDQ} has opposite sign for each pair, their outputs are the same. Since B_{EARTH} has the same sign for both sensors, their outputs cancel.

Constant or slowly-changing external fields can also be viewed as offsets to the signal. As long as they are small enough to permit stochastic sensor operation, the offsets can be canceled by delta I_{DDQ} techniques. In practice, offsets due to device mismatch are much larger than offsets due to external fields.

Fig. 5 also shows that the MAGFET drains are located as close to the supply line as possible, in order to maximize B_{IDDQ}. Once past the notch, carriers cannot be diverted from one drain to the other, so the supply line edge is located at the end of the notch. This configuration further increases MAGFET gain since the carrier velocity rises along the channel, and is highest in the region of

maximum magnetic field. This further increases ΔI since it is proportional to $v \times B$, where v is the carrier velocity.

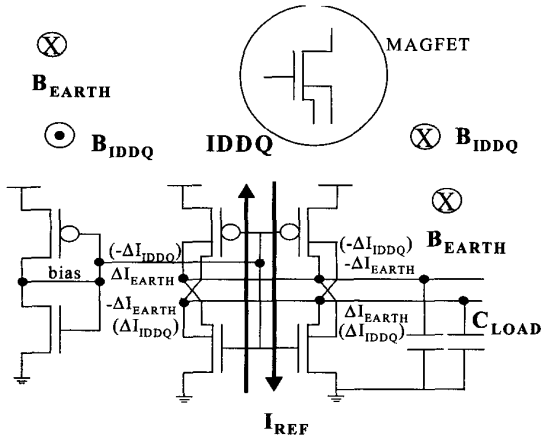

Fig. 4 Paired cross-coupled MAGFET sensor

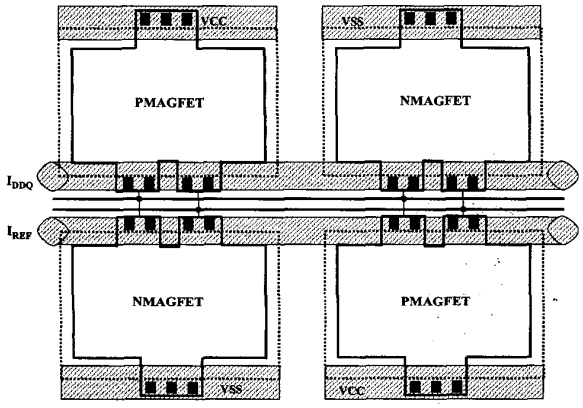

Fig. 5 MAGFET Layout

The noise of a MOS transistor is classified into flicker (1/f) and thermal (white) noise. In section 1.A, we optimized the MAGFET to reduce the flicker noise while keeping the device reasonably small. As discussed in the next section, the SNR is the key parameter that determines I_{DDQ} measurement time. We assume an I_{DDQ} test vector frequency of 1 kHz. So to maximize SNR, we must minimize thermal noise beyond 1 kHz. This is achieved by placing a low-pass filter on the MAGFET sensor outputs. The low-pass filter is formed by the MAGFET output resistance and a MOS capacitor (C_{LOAD}). The corner frequency is set at 1.5 kHz so that it does not significantly attenuate the signal, but blocks most of the white noise, as well as much of the flicker noise. Based on circuit simulation [27], this filter reduces the RMS noise value by 13 times, to 100 μV.

D. Stochastic Sensor

Despite the efforts to improve the MAGFET sensor, the MAGFET signal and SNR is too small to amplify by traditional analog means. For a 10 μA I_{DDQ} level, the MAGFET output will be about 0.33 μV and the SNR about 1/300. Analog data acquisition in combination with digital signal processing can be used to amplify such signals [28], but would take too much chip area. To achieve high resolution to detect small signals, the digitizing decision must be shifted as close as possible to the measurement location in order to avoid additional noise. This can be achieved in a single stage by using a flip-flop initialized to its metastable state, as shown in Fig. 6. The signal is compared with the background noise to determine whether the flip-flop should resolve to a "0" or a "1". Thus this circuit operates when the signal is smaller than the noise. The signal is repeatedly measured, and the resulting digital bit stream is fed into a counter in order to form an ADC.

The circuit in Fig. 6 operates in the following manner. When the clock is low (clockb is high), the two flip-flop nodes equalize to an intermediate voltage. When the clock rises high, the flip-flop goes into the metastable state. Noise will flip it one way or the other. The calibration circuit ensures that when no input is present, the flip-flop has equal probability of flipping one way or the other. The differential MAGFET inputs (In and Inb) causes a slight imbalance on the nodes, biasing the flip-flop decision. The positive feedback provides very high gain. Such a decision is very fast. In a 180 nm technology, the flip-flop should operate well above 1 GHz.

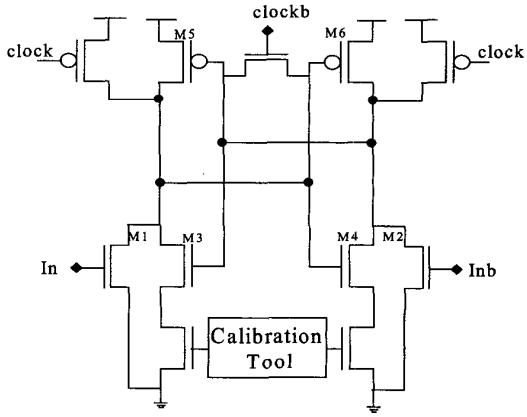

Fig. 6 Stochastic sensor

Stochastic analysis is based on the stochastic evaluation of binary data coming from the binary decisions made when the flip-flop compares the input signal with random noise [20]. If no input signal is present, the difference in node voltages Δv is transistor noise with a Gaussian distribution with mean zero and standard deviation σ. The value of Δv at the start of the decision process determines whether the flip-flop flips to a "0" or a "1". Since the mean is zero, the deviation from equal probabilities for "0" or a "1", ΔP, is zero.

The number of flips to a "1" (S) follows a binomial distribution since each flip-flop decision is independent. For n decisions, the difference b between "1" and "0" counts (e.g. as computed by an up/down counter) has mean $b = 2S - n$, *and range* $-n < b < n$. The probability distribution of S is:

$$P(S) = \binom{n}{\frac{b+n}{2}} \left(\frac{1}{2}+\Delta P\right)^{\left(\frac{b+n}{2}\right)} \left(\frac{1}{2}-\Delta P\right)^{\left(n-\frac{b+n}{2}\right)}.$$

For large n and small ΔP, the binomial distribution for b can be approximated as Gaussian:

$$P(b) \approx \frac{1}{\sqrt{2\pi n}} \exp\left[-\frac{1}{2}\frac{(b-2n\Delta P)^2}{n}\right].$$

When a signal is present, Δv will be the difference between the noise v_N having mean zero and standard deviation σ, and the signal v_B. The decision-producing probability distribution function is given by:

$$P(v) \approx \frac{1}{\sigma\sqrt{2\pi}} \exp\left[-\frac{1}{2}\left(\frac{\Delta v}{\sigma}\right)^2\right]$$

$$= \frac{1}{\sigma\sqrt{2\pi}} \exp\left[-\frac{1}{2}\left(\frac{v_N - v_B}{\sigma}\right)^2\right].$$

A small probability deviation ΔP from 0.5 is expressed by the following integral:

$$\Delta P = \frac{1}{\sigma\sqrt{2\pi}} \int_{v=0}^{v_N} \exp\left[-\frac{1}{2}\frac{(v-v_B)^2}{\sigma^2}\right] dv$$

Accordingly, the response of a stochastic sensor follows a Gaussian cumulative density function around the metastable point. This can be approximated as linear when the signal is much smaller than the noise as shown in Fig. 7. The probability of getting a "0" or "1" output from the flip-flop represents the equivalent magnitude of the analog input signal. The sign relative to 0.5 indicates whether the input is positive or negative (e.g. the direction of current flow). The probability is not affected by the noise since it has zero mean [29]. Supply noise is common mode and so also does not affect the probability. Clock noise is either out of phase and so does not affect the flip-flop decision, or acts as an offset that is handled by the calibration tool. Therefore, the stochastic sensor achieves high sensitivity and high noise immunity through repetitive operation.

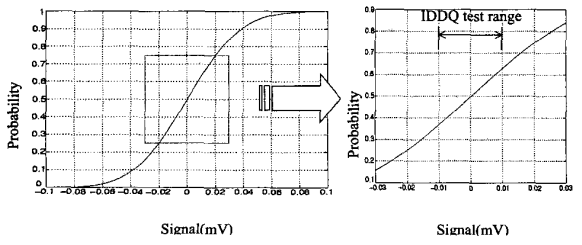

Fig. 7 Transfer characteristic of stochastic sensor

Since stochastic analysis is a sampling process, the number of samples n must be determined to achieve the desired measurement resolution. The estimate of the input v_B follows a t-distribution, and so has a 1 - α confidence interval about the mean of approximately:

$$\pm\frac{Z_\alpha \sigma}{\sqrt{n}}$$

The maximum allowable error in our estimate of v_B with probability 1 - α is defined as $E \geq Z_\alpha \sigma/\sqrt{n}$. The sample number to meet this requirement is:

$$n \geq \left[\frac{Z_\alpha \sigma}{E}\right]^2$$

In our application, we can replace E and σ with the required resolution and the RMS noise value. Z_α is determined from a t-distribution table based on the desired confidence level [30]. Rewriting, the required number of samples is:

$$n \geq \left[\frac{Z_\alpha}{v_B/\sigma}\right]^2 = \frac{Z_\alpha^2}{SNR^2}$$

Therefore, the number of samples to estimate the signal by stochastic operation is critically dependent on the SNR. Fig. 8 shows the number of repetitions for a stochastic sensor for different confidence levels and SNR. Our sensor system has an SNR of about 1/300, which indicates 350 000 to 1 500 000 samples to achieve the desired confidence level.

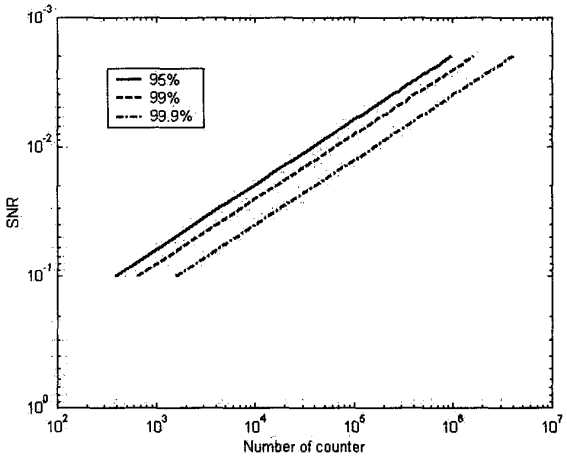

Fig. 8 Number of repetitions of stochastic sensor

Both n and the clock frequency determine the total test time for one I_{DDQ} test vector. Given n as determined above, the clock rate must be maximized to achieve minimum test time. For n = 1 000 000 and a 1 ms test time, the clock frequency must be 1 GHz. The clock frequency is closely related with the flip-flop resolving time, which is the required time to leave the metastability region. If the clock frequency is too high, the sensor will have a high

probability of remaining in the metastable state. This is equivalent to a "don't know" output rather than a "0" or "1" and biases the output value towards zero (since the counter does not count). To improve the resolving speed in a given technology, we use a two-stage pipelined stochastic sensor, with each stage operated during the opposite clock phase. Using this two-stage approach, the available sensing time of the stochastic sensor becomes twice that of a single-stage sensor, permitting higher operating frequency without introducing errors. In a 180 nm technology, circuit simulations show that the stochastic sensor should easily operate at over 1 GHz.

Distributing a 1 GHz clock to many BICSs is a challenging design task. However this problem is simplified because there is no need for BICSs to operate in phase. This permits stochastic sensor clocks to be generated by regional clock generators, triggered by a central control signal.

E. Reference Current

In the MAGFET layout, a second wire runs in parallel with the supply line, either next to it as shown in Fig. 5, or directly above or below. This wire is used to supply a known current, and thus a known magnetic field to the MAGFET. It is termed the I_{REF} signal. It has a number of uses in calibration, testing, and diagnosis.

1. Gain Calibration

The counter value is a function of both the signal and the SNR. The higher the SNR, the higher the counter value for a given signal. In order to translate counter values into I_{DDQ} values, the gain must be measured, and used to externally correct the counter values. The gain can be measured by placing a step change in the current on the I_{REF} line and measuring the change in the counter value. No vectors are applied to the chip during either measurement so that the I_{DDQ} remains stable. Note that if setting I_{DDQ} pass/fail thresholds based on the distribution of vector values, knowledge of the gain is not necessary since the measurements are normalized (e.g. Z-transformed) before analysis.

2. Single Threshold Reference

During testing, the I_{REF} line can be set to a single threshold current I_{TH} in the opposite direction from the supply current. This value is estimated or determined empirically. In effect this threshold current is subtracted from the I_{DDQ}. If the I_{DDQ} is much below this threshold, the counter value will be substantially below *n/2*. If the I_{DDQ} is much above the threshold, then the counter value will be significantly above *n/2*. This can be used to easily determine a single pass/fail threshold current for all sensors on the chip.

3. Resolution Enhancement

The counter size limits the value of *n* and thus the measurement resolution. In addition, the transfer characteristic of the stochastic sensor is nonlinear when the signal is large. Using I_{REF} to subtract the expected average I_{DDQ} value can increase the I_{DDQ} sensor system resolution. The sensor will measure the difference from I_{REF}. If the sensor-to-sensor I_{DDQ} variation from I_{REF} is small, a larger value of *n* can be used before counter overflow. For an individual sensor, very high resolution can be obtained by doing binary search with the I_{REF} value. This is useful during process characterization and defect diagnosis.

I_{REF} can be supplied externally to all BICS, or it can be internally generated on a regional basis. Several different values can be generated to provide higher resolution or increased flexibility.

F. Self-Calibration

Even though the stochastic sensor achieves high gain, high resolution and noise immunity, it is vulnerable to offset voltage due to device mismatch. Due to the high gain, even a very small mismatch in the MAGFET sensor or stochastic sensor will affect the resolution or exactness of the I_{DDQ} measurement. Furthermore the offset values that commonly occur are much larger than the signal or noise levels, which causes the counter output to be 0 or *n*. In effect, such offsets place the stochastic sensor to one of the extreme ends of its transfer characteristic curve. The stochastic sensor must be calibrated to minimize these offsets prior to I_{DDQ} measurements. On-chip self-calibration is used so that many BICSs can be calibrated in parallel on a chip. The self-calibration tool corrects for any offset in the stochastic sensor or MAGFETs by adjusting the bias voltage on the pulldown transistors of the first flip-flop, as shown in Fig. 9. The gain of the first flip-flop is sufficient that the second flip-flop does not need calibration. The bias voltage is generated using a charge pump as shown in Fig. 9. So as to maintain the bias voltage over a long period of time (e.g. 1 second) and to achieve higher resolution, complementary MOS storage capacitors are attached to the bias nodes. Complementary capacitors are used so that leakage currents cancel out. A startup circuit triggered by a PWRUP signal is used to quickly set the bias voltage to approximately $V_{DD}/2$ prior to the start of calibration.

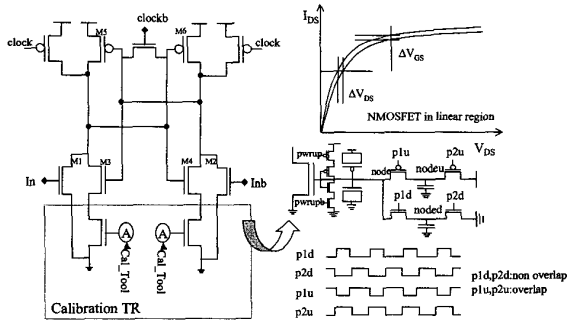

Fig. 9 Self-calibration tool and charge pump operation

Self-calibration is done digitally by integrating each cycle result over the given calibration interval. During calibration, the input signal is shut off and the flip-flop operates continuously, with the CALB signal high. Each

flip generates a charge pump signal through the pumping clock generator to create an opposing change to the bias voltage of the calibration transistor (M). The pumping transistors and calibration capacitors are sized so as to give high calibration resolution. Typically n calibration cycles are performed. Initially the flip-flop always flips the same way, causing the opposing bias voltage to quickly bring the flip-flop into the stochastic operating range.

Self-calibration provides the following benefits:

- Cancels offset in the MAGFET sensor and stochastic sensor.
- Improves sensitivity by shifting the dynamic range so that the stochastic sensor operates in the linear region.
- Provides auto-zero compensation for low-frequency noise.

There are two primary limitations to how long the BICS will stay in calibration:

- Unbalanced leakage or noise injection on the bias voltage storage capacitors.
- Circuit drift due to temperature or voltage change.

The calibration circuit presents two primary system challenges. Both stem from the need to shut off the signal during calibration. This requires shutting off the I_{DDQ}, which requires powering down the circuit under test. In some designs this can be down with a power switch, but more commonly the entire circuit must be powered down, and then later reinitialized. This requires that the circuit under test and the BICS have separate power supplies. The second challenge is that if all I_{DDQ} tests cannot be completed before the BICS goes out of calibration, the chip must be powered down, recalibration performed, and then powered back up again. This is relatively quick if all state is stored in scan chains, but could require long reinitialization times for highly-sequential circuits. To avoid this, our design goal is that the BICS can be calibrated once at chip power-up, and then all I_{DDQ} tests can be completed before recalibration is necessary. We believe that a calibration holding time of 1 second is sufficient for this.

G. Scan Chain and Counter

The stochastic sensor result is accumulated in a counter and scanned out of the chip. To minimize the transistor count, we combine the counter and scan chain together as shown in Fig. 10. Accordingly, the counter and scan chain have two operation modes – counter mode and scan mode. In counter mode, the SCAN/SCANB signals are kept low/high respectively, while Q1/Q2 is kept low/high. It operates as a ripple counter. The advantages of a ripple counter are that it is simple, fast, and uses relatively low power since most activity is in the first few stages. Since it is not operating in the metastable region, it should easily be able to keep up with the stochastic sensor.

During scan mode, SCAN/SCANB are high/low and Q1/Q2 are toggled to generate non-overlapped clocks. The non-overlapped signals Q1/Q2 shift the counter result. In Fig. 10, INV_L is a weak inverter that acts as a data holder during scan operation. Due to the extra capacitive loading of the counter logic, the scan chain should operate at a slightly lower frequency than a normal scan chain. However typically scan chain frequency is limited by the clock distribution.

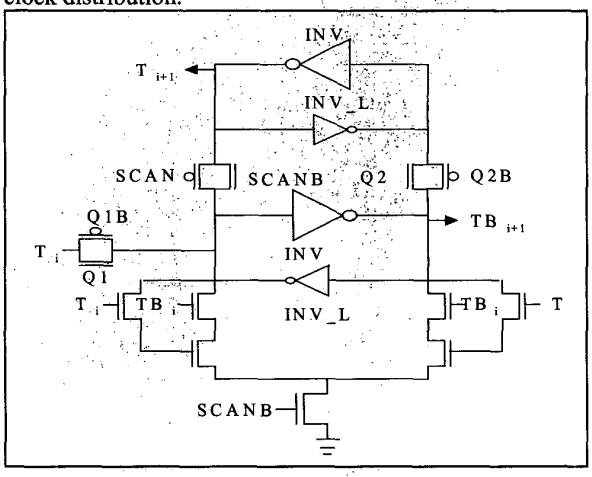

Fig. 10 Counter and scan chain

An example scan chain connection using the proposed I_{DDQ} sensor is shown in Fig. 11. The scan chains of all the BICS are connected to form one long chain. Since the scan chain is a larger fraction of the BICS area, its overhead can potentially be reduced by providing a parallel load capability, and using it as a regular scan chain during scan test. That option is not explored in this work.

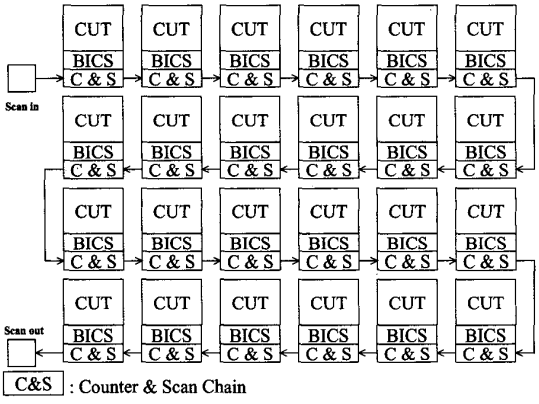

Fig. 11 Scan chain map within chip

The size of the counter/scan chain depends on the number of counter bits N required for the desired resolution. The number of bits is $N = \lceil \log_2 n \rceil$ where n is the number of stochastic sensor clock cycles, or 20 bits for 1 000 000 clock cycles. More precision can be achieved with fewer bits by counting until the counter is full, then shifting its results out (and shifting zeros into the counter), and then resume counting. However this can be relatively

slow for typical scan chain lengths, and lengthens the time required for the BICS to stay in calibration.

3. I_{DDQ} Sensor Operation

The operation of the proposed I_{DDQ} sensor is divided into five different operating modes: power-up, calibration, scan-in, measurement and scan-out. During power-up mode, every node of the sensor system is stabilized and ready for self-calibration. Only after power-up enable (PWRUP), external signals can be accepted and the next mode (self-calibration) starts. Self-calibration is performed until it is terminated by the CALB signal. During scan-in mode, the counter is reset by scanning in zeros. The scan-in operation is initiated by the non-overlapped scan clocks Q1/Q2. The normal measurement mode is initiated following the scan-in mode while disabling every control signal except clock/clockb signals. In scan-out mode, the measurement results are scanned out serially using the counter/scan chain operating as a shift register.

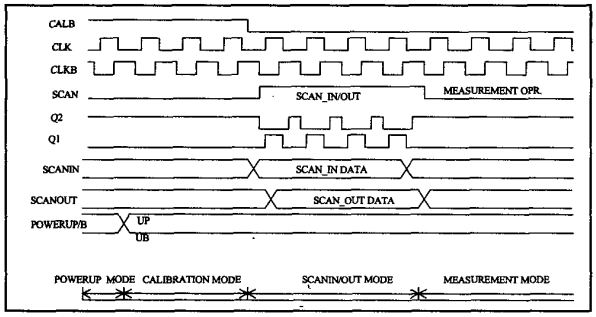

Fig. 12 BICS Timing diagram

Fig. 1 and Fig. 12 show the block diagram and the timing diagram of the proposed sensor system respectively. In this timing diagram, scan-in/out mode is done at the same time. While shifting the counter result to the SCANOUT pad, the counter and scan chain shifts "0" in from the SCANIN pad at every Q1/Q2 clock to reset the counter to "0". During measurement mode, the counter mode of counter/scan chain will be on and act as a counter accumulating results from the stochastic sensor.

We calculate the total test time for each test vector by summing the scan-in time and stochastic sensor measure time. The test time per vector is $\#CUT \cdot N \cdot t_{SCAN} + n \cdot t_{CLK}$, where $\#CUT$ is the number of circuit partitions, N is the number of counter bits, t_{SCAN} is the scan cycle time, t_{CLK} is the stochastic sensor cycle time, and n the number of stochastic sensor clock cycles. This assumes that all BICSs are configured in one long scan chain and no other scan registers are part of the chain. For $n = 1\ 000\ 000$, $N = 20 = \log_2 n$. Assuming $t_{SCAN} \approx t_{CLK}$ due to clock routing, the total vector time is $t_{SCAN} \cdot (\#CUT \cdot \log_2 n + n)$. Assuming a 50 MHz clock and 100 CUTs, I_{DDQ} vectors can be applied every 20 ms, not counting voltage sensitization vector time.

4. Experimental Results

A series of BICS test chips was designed and fabricated, in order to evaluate different circuit and layout options, and verify circuit operation and performance. The most recent test chip shown in Fig. 13 was fabricated in 180 nm technology at Texas Instruments. The chips included individual MAGFETs, several different MAGFET designs (with *W/L* values of 35/50, 70/100, and 140/200 in microns), designs with external access to the stochastic sensor, different stochastic sensor designs, and separate 22-bit up and down counters. The chip includes 13 cross-coupled MAGFETs, 8 stochastic sensors and 8 counter/scan chains. Additionally, separate MAGFETs are included to measure the MAGFET DC characteristics.

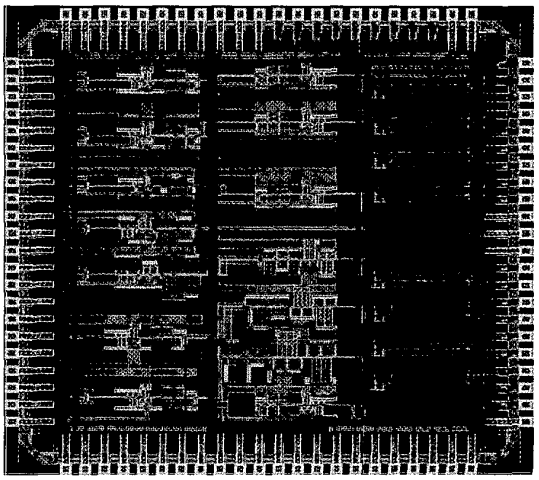

Fig. 13 Test chip layout (0.35 mm x 0.35 mm)

Two power rails are used to separate the main power for sensor operation from the quiet power for the MAGFET sensor. Note that this is only a precaution and measurement convenience since power supply noise is common mode and should not significantly affect sensor operation. Two external current sources, I_{REF} and I_{DDQ}, are used to supply the reference source and the measurement source. In the most recent chip, each of the 13 MAGFET sensors is connected to their output pads through a buffer that shows nearly constant gain (0.85) over the operating range around $V_{DD}/2$. This buffer prevents the MAGFET operation from being interfered with by I/O pad circuitry or tester leakage.

DC characteristics of MAGFET sensors were measured using a HP 4156 parameter analyzer. Fig. 14 shows the MAGFET DC gain, with 64 measurements averaged to reduce the noise level. The slope of the inserted equation of ΔV vs. I_{DDQ} shows the MAGFET sensitivity in voltage form. Considering the buffer gain of 0.85, the actual MAGFET gain is 1.36 μV/100 μA. This is about 2.2 times lower than simulation. We believe this is due to the simple MAGFET model used during simulation.

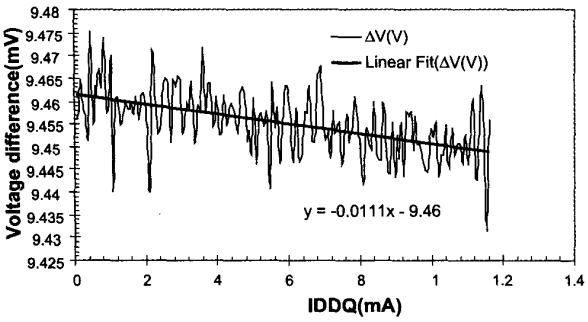

Fig. 14 DC characteristic of MAGFET

The complete stochastic sensor operation was verified. A differential voltage was forced onto the inputs of the flip-flop, and stochastic sensing was done with self-calibration. Due to tester limitations, the scan and sensor clocks were run at only 10, 20 and 50 MHz. At these slow clock rates, miscounting due to metastability did not occur, in that the up and down counters always summed to the number of clock cycles applied. Measurements were taken using 2^{19}, 2^{20}, and 2^{21} clock cycles.

The self-calibration tool was tested by comparing stochastic sensor results with calibration on and off. Without calibration, even an input difference of 10 mV will not cause stochastic operation, indicating that flip-flop circuit mismatch is greater than this. When calibration was performed for 2^{19} or more clock cycles prior to measurement cycles, stochastic behavior was observed. Fig. 15 shows the transfer curve of a sensor when run at 50 MHz for 2^{19} clock cycles. The measurement is done 64 times and then averaged to minimize sampling noise. Calibration was performed before each measurement. The measured gain of the stochastic sensor is the slope (ΔCounter value/V) of the transfer curve. The slope around the origin is 300 counts per microvolt. In comparison, the counter sampling noise has a 95% confidence interval of +/- 724. Combined with the MAGFET gain, this suggests a lower bound on stochastic sensor resolution of about 180 μA. The stochastic sensor gain is much lower than predicted since its noise level is higher than expected.

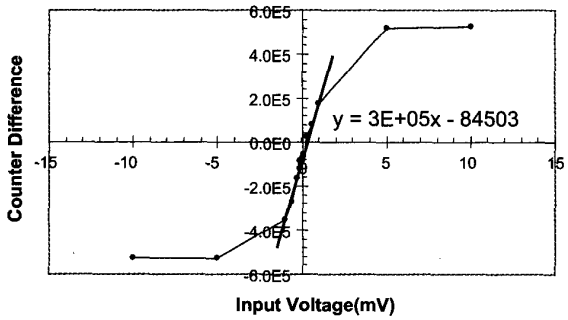

Fig. 15 Measured characteristic of stochastic sensor

For a zero input signal, the counters had a standard deviation of approximately 20 000. This is much more than the 362 predicted by sampling theory and indicates a very high noise level. The simulation results in Fig. 7 show that a ± 100 μV input signal should saturate the counters, indicating a noise level considerably lower. Extrapolating from Fig. 15 gives an RMS noise level of about 1.75 mV, about 20 times larger than expected. As described below, this "noise" is really caused by shortcomings in the calibration tool combined with tester limitations.

A key parameter of interest is how long the BICS will remain in calibration. This was tested by first calibrating the circuit with a zero input signal. Then a measurement was repeated a number of times, and the drift in counter values observed. The counter difference values begin drifting from the small value close to 0 to the maximum value *n*. The time between measurements was carefully observed for measurements of 2^{19}, 2^{20}, and 2^{21} clock cycles. The overhead of the workstation host on the tester is about 80 ms, so each measurement takes about 100 ms. Fig. 16 shows the counter difference deviation as a function of the time elapsed since calibration for three different stochastic sensors. As can be seen, all of the sensors go out of calibration quickly, and completely leave the stochastic range in less than a second.

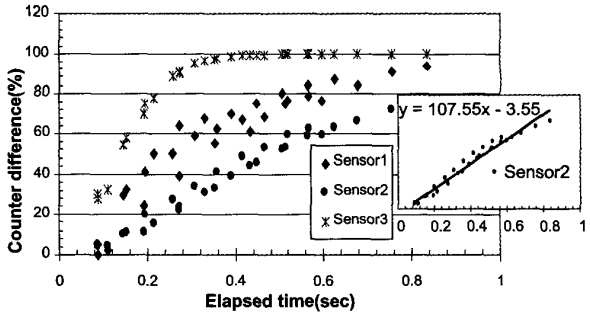

Fig. 16 Calibration validation

Sensor 2 had the lowest drift rate, and its offset exceeds the sampling noise for 2^{20} measurement clocks within 34 ms. Sensor 3 is already outside the range of the MAGFET input signal before the first measurement is taken. The variation in the measurement time due to the software-based tester in combination with the drift introduces a low-frequency noise source into the measurements that is far larger than any other noise source. This is the noise source observed during stochastic sensor measurements that is about 20 times larger than the white and 1/f noise sources. It introduces an offset and reduces gain. If it did not drift, the offset could be removed by delta-I_{DDQ} testing. Unfortunately the stochastic sensors directly hooked to MAGFETs have high drift rates. The maximum I_{DDQ} that can be supplied to the test chip is about 10 mA, and the resulting MAGFET output is too small to be detected by the stochastic sensor in the first

measurement following calibration. The observed output is the calibration noise, not the MAGFET signal.

The reason that the calibration circuit drifts much faster than expected is that the charge pump transistors leak far more than expected, and the mismatch between the pullup and pulldown leakage is sufficient to cause the storage capacitor voltages to drift much faster than expected. The leakage can be reduced by several orders of magnitude by switching to the high-threshold option for these transistors, using a longer channel length, and a cascode arrangement, and reducing the gain of the calibration circuit to make it more insensitive to drift. This will be sufficient to achieve the one-second calibration hold time goal while still achieving good initial calibration.

The short-term options to get around the calibration problem are to use a faster tester, rewrite the test program to do both calibration and measurement within the same vector sequence, or to cool the chip to reduce transistor leakage. Unfortunately none of these options is currently available to us. Therefore we are designing a fifth test chip. This chip will also correct some circuit errors that had to be corrected via focused ion beam to enable testing.

5. Conclusions

In this research we have outlined the requirements for I_{DDQ} testing of future technology generations and shown that built-in current sensors are the only solution that scales with technology. We have developed a BICS approach that meets the requirements, and designed and fabricated a series of test chips. We have verified the individual BICS components, but could not test the MAGFET directly feeding the stochastic sensor since the calibration hold time is too short for the available tester. We are designing a new test chip to correct this problem, and expect it to achieve our goals.

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