Improved Wafer-level Spatial Analysis for I_{DDQ} Limit Setting

Sagar Sabade D. M. H. Walker

Department of Computer Science
Texas A&M University, MS 3112
College Station TX 77843-3112
Tel: (979) 862-4387
Fax: (979) 847-8578
E-mail: {sagars, walker}@cs.tamu.edu

Abstract

This paper proposes a new methodology for estimating the upper bound on the I_{DDQ} of defect free chips by using wafer level spatial information. This can be used for I_{DDQ} pass/fail limit setting. This methodology is validated using SEMATECH data. Such a methodology accounts for the change in I_{DDQ} due to process variations across wafers and reduces false rejects resulting in yield loss. Typical scenarios in using this approach are discussed. The results are compared with traditional methods.

1. Introduction

CMOS circuits consume very little power when the inputs are stable, as both p-type and n-type transistors do not conduct simultaneously. Thus the quiescent current in CMOS circuits (denoted by I_{DDQ}) is typically low. Any appreciable increase in the quiescent current, therefore, indicates the likely presence of a defect (e.g. a bridging fault). I_{DDQ} testing has been successfully employed to screen defective ICs or ICs having reliability hazards [1,2]. In the deep sub-micron (DSM) era, however, the leakage current is increasing and it has become difficult to distinguish between higher current due to a defective chip and a high I_{DDQ} process corner [3,4]. This paper discusses a new approach for defining the pass/fail threshold based on information about neighboring dice on a wafer. This approach was validated using SEMATECH data[1]. This paper is organized as follows. In section 2, we describe the problem of setting the pass/fail limit for I_{DDQ} and discuss the motivation to solve this problem. In section 3 we discuss the philosophy behind using neighboring die information. Section 4 details the methodology of using such information and some particular cases that are encountered. Section 5 presents the results observed for SEMATECH data. The last section concludes the paper.

[1] This data comes from the work of the Test thrust at SEMATECH, Project S-121 on Test Methods Evaluation. The results and analysis presented here are our own and do not necessarily represent the views of SEMATECH or its member companies.

2. Motivation

I_{DDQ} testing has been a very effective test method. It offers high fault coverage with a small set of test vectors [5]. The traditional approach has been to define a maximum permissible value for I_{DDQ}, called "I_{DDQ} Threshold", I_{th}. All chips having a vector with I_{DDQ} higher than I_{th} are considered likely to be defective and are either rejected or subjected to burn-in test. All chips that have I_{DDQ} lower than I_{th} are said to have passed the I_{DDQ} test. The I_{DDQ} test when combined with a voltage test and/or speed test provides an effective way of separating defective chips from the good ones [6].

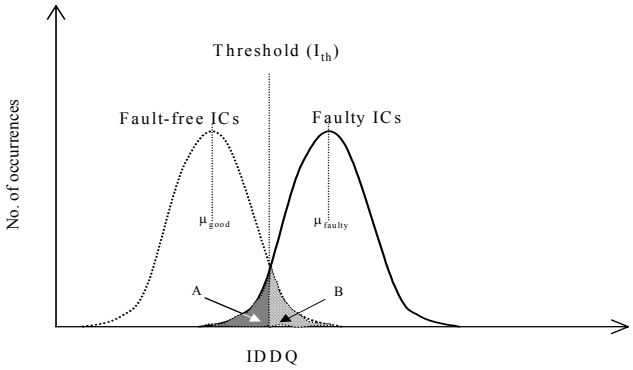

Figure 1: Typical I_{DDQ} distributions

As transistor geometries are scaled down, the leakage current increases exponentially [3]. As the normal value of I_{DDQ} increases, it becomes difficult to distinguish faulty chips from the good ones. This problem is further worsened by an increase in die-to-die, lot-to-lot and wafer-to-wafer variations in I_{DDQ}. A typical distribution of I_{DDQ} values is shown in Figure 1. There are dice that pass I_{DDQ} test but are defective (region A in Figure 1) and dice that fail I_{DDQ} test but are good (region B in Figure 1). While rejecting a die that passes all other tests but I_{DDQ} (region B)

causes yield loss, letting a die pass just because it has passed I_{DDQ} test (region A) can result in a customer return. Therefore, semiconductor manufacturers need to define metrics for I_{DDQ} pass/fail decisions very carefully.

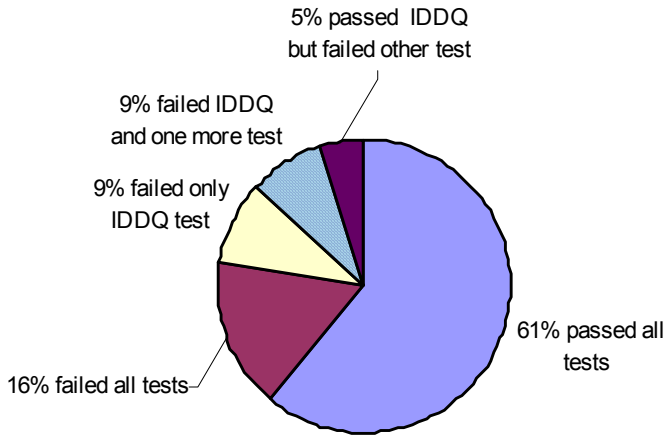

Figure 2: SEMATECH test result breakdown

The SEMATECH experiment was conducted to evaluate the relative effectiveness of functional, stuck-at, I_{DDQ} and delay tests. The test vehicle used was an IBM graphics controller chip. It was a fully complementary CMOS design of approximately 116K ASIC standard cells with effective and drawn channel lengths 0.45 μm and 0.8 μm, respectively [7]. A sample of 18 466 chips was tested at wafer and package level [6]. For each chip a total of 195 I_{DDQ} measurements were taken. If any of these readings exceeded a threshold of 5 μA, the die was considered an I_{DDQ}-fail. This I_{DDQ} threshold did not necessarily represent a good manufacturing limit. The breakdown of the test results of these dice is shown in Figure 2. As shown, out of 18 466 dice, 3040 (16%) failed all the tests at wafer probe. Of the remaining 15 426 dice, 11 263 (61%) passed all the tests and 1689 (9%) failed only I_{DDQ} test, 1619 (9%) failed I_{DDQ} and at least one more test and only 855 dice (5%) failed other than I_{DDQ} test at the wafer level. The relationship among test failures is shown in Figure 3. Notice that a high percentage of dice are I_{DDQ}-only fails.

After wafer probe, a sample of all dice were packaged, tested and then subjected to six hours of burn-in and tested again. We consider a die that tested good before packaging to be good even if it failed after packaging. This result can be attributed to a packaging defect. Of the I_{DDQ}-only failed dice at wafer probe, 1511 (89%) failed only I_{DDQ} test after burn-in, while only 47 dice (3%) failed at least one more test. The post burn-in results are not available for the remaining dice. This clearly indicates that rejecting a die based on a static threshold I_{DDQ} test can result in considerable yield loss. This justifies the need of setting an appropriate value of the current threshold (I_{th}) to minimize yield loss as well as test escapes.

Various approaches have been suggested to solve the I_{DDQ} limit-setting problem [8]. They either follow a model-based approach [9,10,11] or an empirical approach [12]. The basic idea is to reduce the variance of the I_{DDQ} distributions of good and faulty chips so as to reduce the overlapping area between them. This is to make the defect manifest itself by increasing the signal to noise ratio (SNR) of the I_{DDQ} measurement.

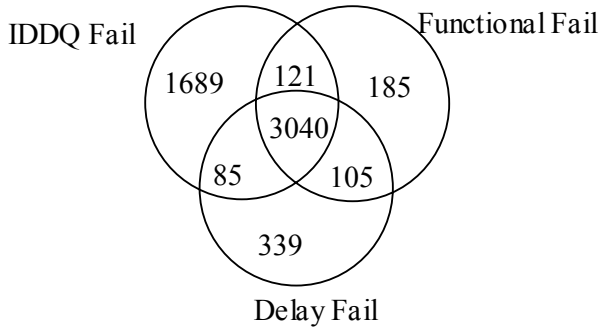

Figure 3: SEMATECH failed chip relationships

The current signature approach [13] relies on arranging all I_{DDQ} values in increasing order. It is suggested that the presence of a defect should result in a "step" in the current signature, instead of a gradual change as in the case of a good IC. To be effective, this approach needs an appreciable number of measurements. Unfortunately, I_{DDQ} is a slow testing method. Thus, it is not practical to take many measurements for each die unless a special sensor is used [14].

Delta-I_{DDQ} takes the difference between two adjacent I_{DDQ} values [15]. It is observed that per-die ΔI_{DDQ} has smaller variation than the original measurements. This scheme is further improved in [16]. The ΔI_{DDQ} technique is observed to be more effective than traditional I_{DDQ} test [17].

The current ratio technique [18] relies on the idea that in spite of the variation in I_{DDQ}, the ratio of the maximum and minimum I_{DDQ} values should remain the same for all chips.

A statistical clustering method has been reported in [19]. This method clusters chips using I_{DDQ} measurements. It is suggested that good and defective chips will be clustered separately. The threshold value can then be refined by using the cluster data.

3. Using Neighboring Die Information

It is known that defects tend to appear in clusters. Thus a die that passes all the tests and is surrounded by defective dice on a wafer is more likely to be defective (i.e. a test escape) than a die which is surrounded by good dice. It was suggested [20,21] that the probability of failure of a die could be related to the test results of its neighboring dice on the wafer. The Wafer Oriented Test Evaluation (WOTE) technique was validated using SEMATECH data [22]. We propose a methodology to determine the I_{DDQ} pass/fail limit

by measuring I_{DDQ} values of the neighboring dice. A simple scheme uses the average of the I_{DDQ} values of the neighbors [23]. This approach is expected to give a higher threshold if many neighbors are defective and have elevated I_{DDQ} values. To give less weight to the outliers a better scheme would be to use the median I_{DDQ} values. A variation of the ΔI_{DDQ} scheme may be employed to take the difference between I_{DDQ} readings of the center die and its neighbors. Another possible method is to use X-Y information and estimate the gradient of I_{DDQ} in this region of the wafer. Estimating the process gradient in local wafer regions has been shown to improve the prediction of microprocessor clock speeds [24, 25]. This method is described in the next section.

4. Limit Setting Approach

There are eight neighboring dice for a non-edge die on a wafer. For each fully functional die in the SEMATECH data, we define a 3-D plane for each I_{DDQ} vector using X and Y coordinates on the wafer and I_{DDQ} value as the Z-coordinate. The plane is formed using linear regression using the least squares fit method [26]. The details are provided in Appendix A. The center die readings are not used while forming the plane to eliminate bias. Also, typically in a practical test environment I_{DDQ} data is not available for functional fails. Therefore dice that failed a voltage test are not used for plane formation. Figure 4 shows readings for a wafer as projections on the XY plane. Notice that some areas of the wafer have high frequency spatial variation. The dice having extremely high I_{DDQ} (e.g. several mA) are gross outliers. These gross outliers are eliminated using a statistical technique described later. Figure 5 shows these I_{DDQ} projections after gross outliers are eliminated. Notice that appreciable high frequency spatial variation still remains. The projection off the graph near the center of the plane is for a die (called die B below) that has I_{DDQ} of more than 2 μA but less than 5 μA. If a die has I_{DDQ} considerably higher than its neighbors (i.e. a high-frequency spike) it is likely to be defective. On the contrary, if a die has very low I_{DDQ} compared to its neighbors (a negative spike) it is probable that all the neighbors are defective. This scenario is discussed later.

The use of spatial information gives us insight to understand the impact of process variations on I_{DDQ} and can reduce test escapes. For example, consider the wafer signature shown in Figure 6 (where readings of all dice on a wafer for a vector are arranged in ascending order) for the same readings shown in Figure 5. This is similar to a current signature. A current signature-like approach can detect those failures for which the difference in I_{DDQ} is very high (i.e. high SNR). In Figure 6, the current "jumps" from 2 μA to 6 μA (A to B) and from 6 μA to 12 μA (B to C) are noticeable. Thus the current signature-like approach would reject both the dice B and C. (C is off-scale and not shown in Figure 5). However, die A (the highest value shown in Figure 5) would not be rejected. Observe that in Figure 5, there are quite a few dice, including die A, having I_{DDQ} as low as 2 μA, but exhibiting high spatial frequency. As the current signature does not use spatial information, it cannot distinguish between two I_{DDQ} failed chips, one surrounded by faulty chips and the other surrounded by good chips. It is likely that the former chip is good and exhibits high I_{DDQ} owing to a leaky wafer region. The current signature approach would treat them the same way and reject both.

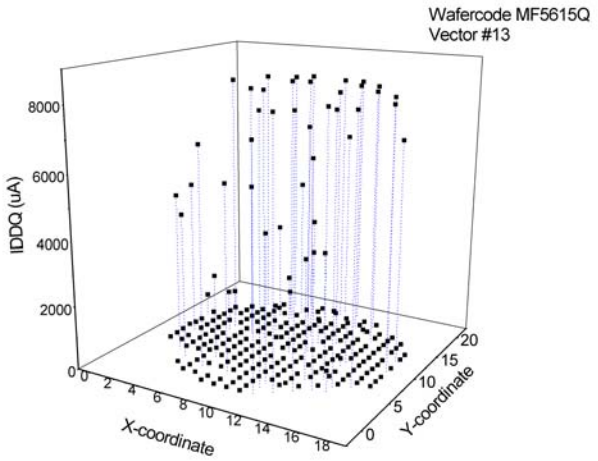

Figure 4: I_{DDQ} projections on XY plane

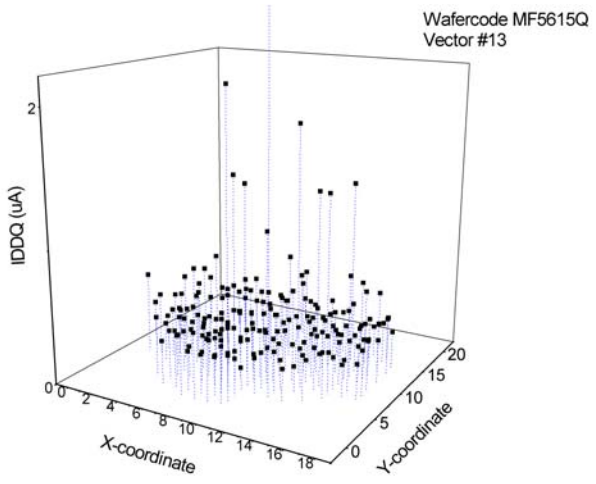

Figure 5: IDDQ projections after outlier removal

At least three points are needed to define a plane. As shown in a typical wafer map (Figure 8), this is not possible for some dice on the edge of a wafer or in a region of low yield. Also, some dice may not have information about all neighbors. Such dice are considered to be potential candidates for burn-in. Alternatively, dice at longer distances can be used for prediction [23]. Unless outliers are rejected, this can bias the data point (even if the neighbors are equidistant). Also for larger die this may not be a good estimate.

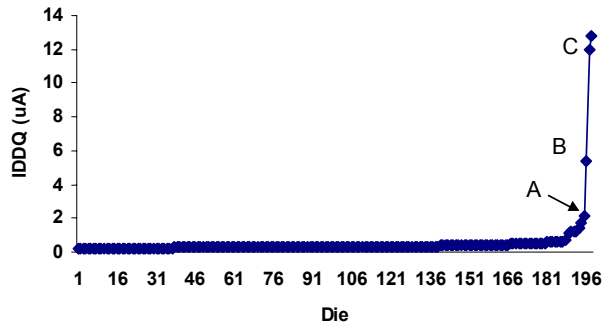

Figure 6: Wafer signature for a vector

Elimination of gross outliers

The gross outliers need to be eliminated before determining the best fitting plane in order to obtain a good estimate of fault-free I_{DDQ}. A global outlier rejection should be used to eliminate maverick lots. The wafer level outlier rejection is needed to eliminate leaky dice. Based on circuit knowledge the approximate fault-free value of I_{DDQ} can be estimated. Alternatively, the wafer median can be used as an indication of fault-free I_{DDQ}. But these do not help reject outliers. There are several ways to reject outliers. Two of them are the Chauvenet's criterion [27] and the Tukey method [28] (see Appendix B).

Since the Chauvenet's criterion (or the Tukey method) is well defined for the Normal distribution, it is important to ensure that the correct distribution is used. The quiescent current depends on various device parameters [29]. The relationship between effective channel length (L_{eff}) and I_{DDQ} is exponential [3]. Since transistor parameters approximately follow a Normal distribution due to process variation, the distribution of fault-free I_{DDQ} can be approximated by the lognormal distribution. We first convert the data to a Normal distribution. The necessary transformations are defined in Appendix C. When applied to I_{DDQ} testing, since outliers are defined only on the higher side, a one-sided Chauvenet's criterion (or Tukey method) must be used. Due to outliers having very high I_{DDQ} and the distribution being skewed towards the right, the Inter Quartile Range (IQR) is very high and thus the Tukey method rejects very few dice. In our analysis, we used Chauvenet's criterion.

Deciding the probability threshold

The most important parameter to be decided while using Chauvenet's criterion is the probability threshold value. A higher threshold would reject many good dice and a lower threshold might keep many bad dice. It may appear that the single threshold problem has remained the same but just changed the domain. However, note that the single threshold method does not use any probabilistic analysis for deciding the threshold. Since the Chauvenet's criterion uses the number of readings for determining the legitimacy of a seemingly outlier reading, it can account for lot-to-lot and wafer-to-wafer variations. A value of 0.5 is normally used [27]. To verify this, we performed a sensitivity analysis of the threshold. The results of the sensitivity analysis are shown in Figure 7. Here overkill was defined as the number of chips rejected by Chauvenet's rejection method that passed all tests (All pass overkill) or failed only I_{DDQ} test (Voltage pass overkill). Note that a tighter threshold rejects good chips while a lower threshold can accept potentially bad chips. The philosophy behind using spatial information is that not all the dice failing I_{DDQ}-only test are bad and not all the dice passing all the tests are good. A threshold of 0.5 was selected because the analysis in Appendix C shows that the results are relatively insensitive for this threshold value. Multiple passes of Chauvenet's criterion should not be applied, as significant information may be lost [30].

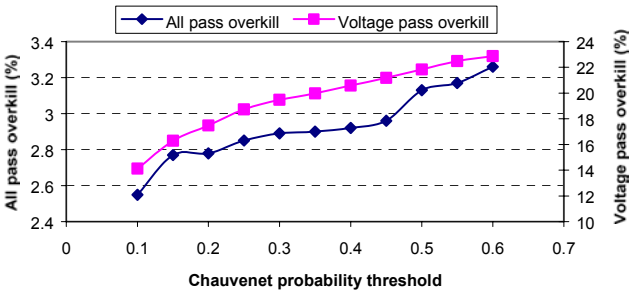

Figure 7: Chauvenet threshold sensitivity analysis

After outlier rejection we perform plane fitting for each vector to obtain the predicted I_{DDQ} value. Each vector is analyzed separately since in general process and defect sensitivity is different for each vector. For a defective die surrounded by good neighbors (non-voltage fails), the plane will be lower than its I_{DDQ} values. On the other hand, if neighboring dice are defective and the center die is good, the plane will be much higher. In this case, however, it is reasonable to expect the center die to be a high risk and a candidate for burn-in.

The predicted plane value is compared with the actual value and the residual is computed for each vector *i* using the following equation

$$R_i = (I_{DDQ\text{-actual}})_i - (I_{DDQ\text{-estimated}})_i$$

We then determine the standard deviation (σ_i) of the residuals across the wafer for each vector. The dice that are above any predicted I_{DDQ} value by more than 3σ are considered high risk and are rejected by our method. In practice such dice would normally be subjected to burn-in. When the center die I_{DDQ} values are below the predicted plane values by more than 3σ, it indicates that one or more of the surrounding dice are likely to be defective. To determine which neighboring dice are indeed defective, we

may need to consider neighboring dice of these dice and follow the same plane prediction-based approach. However, we did not perform this analysis in the present work.

5. Experimental Results

The SEMATECH data was used to validate our approach. We looked at the I_{DDQ}-only failed dice and all test passed dice (codes "1I" and "$$" in Figure 8) and defined planes using neighbor I_{DDQ} values and compared the predicted result with the post burn-in (BI) data. To retain a reasonable sample size, dice where post BI data is not available are not rejected. The complete execution flow of the screening procedure is outlined in Figure 9. Figure 10 shows a projection plot for all the chips that passed the 5 μA single threshold I_{DDQ} test on a wafer. Figure 11 shows the surface plot for the same readings used in Figure 10. Notice that the chips denoted by A, B and C in Figure 10 have I_{DDQ} below 5 μA. However, considering the spatial variation for the wafer, these chips are outliers. In fact, as the surface plot in Figure 11 illustrates, there are high frequency spikes corresponding to these dice.

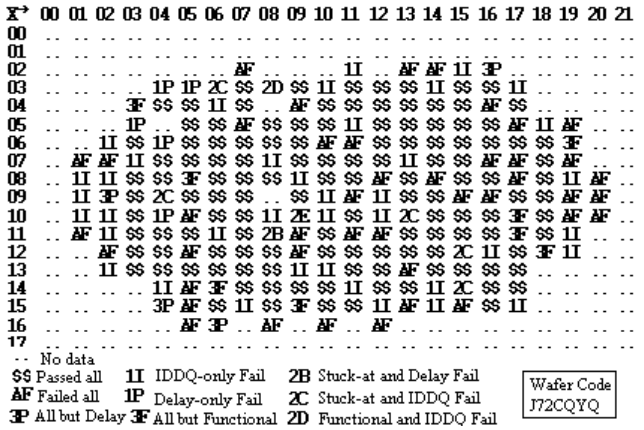

Figure 8: A typical wafer map

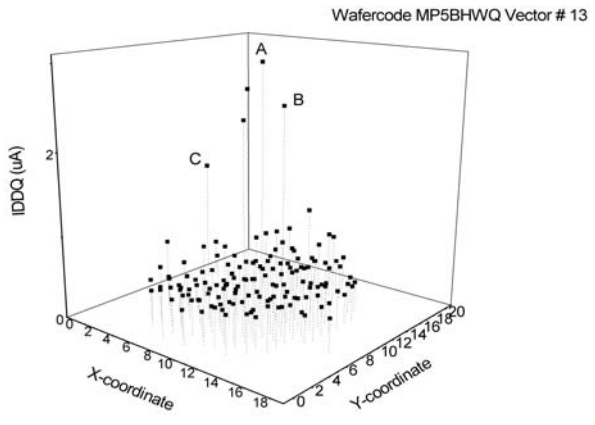

Figure 10: Projection plot for sub-5 μA dice

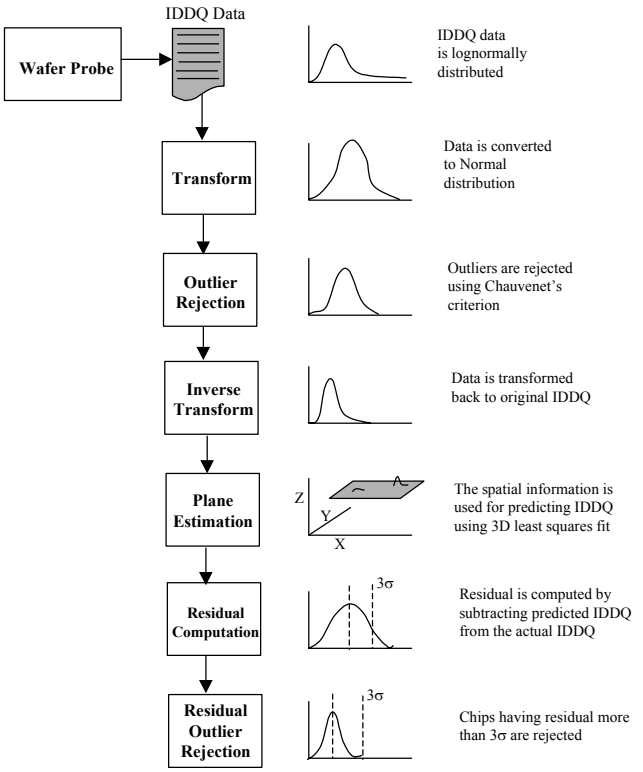

Figure 9: Execution flow of I_{DDQ} screening procedure

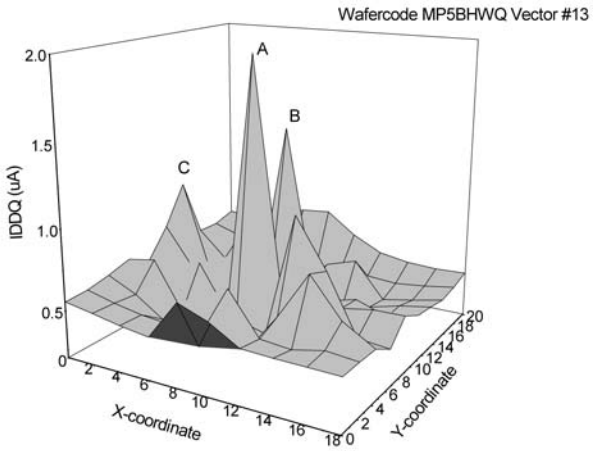

Figure 11: Surface plot for good dice

Table 1 shows a sample of typical cases on a wafer (wafer code MP5BHWQ). This wafer had a total of 197 dice out of which 140 passed all the tests and 21 failed only the 5 μA threshold I_{DDQ} test at the wafer level. Chauvenet's criterion with threshold 0.5 rejected 44 dice out of which 13 failed I_{DDQ}-only test at wafer probe, 28 failed all tests and 3 failed all but functional test. In the accepted dice, 8 dice failed only I_{DDQ} test. Out of these, 4 failed only I_{DDQ} test again after burn-in, one exhibited power failure, and burn-in results were not available for the remaining 3 dice. The

three dice had fewer than three neighbors and could not be predicted using the plane estimate. The number of neighbors that passed all the tests or failed only I_{DDQ} test at wafer probe are listed in the second column, the remaining were either voltage fails or missing. The predicted values and actual I_{DDQ} values are shown for min, max and mean for that particular die across all 195 vectors. Note that the die 1003 predictions are lower than the actual values, as this die is surrounded by all good dice. Similarly, the actual mean for die 0416 is lower than the predicted value. If the difference is large, one must suspect the neighboring dice. One of the neighbors for this die had failed all the tests. It is likely that a defect in this area has affected this die too. The burn-in result is not available for this die.

Table 1: Comparison of predicted and actual I_{DDQ}

Die ID	Pass/ I_{DDQ}-fail	Predicted			Actual		
		Min	Max	Mean	Min	Max	Mean
0316	2/3	2.62	8.44	4.12	4.24	7.36	5.68
0416	3/2	2.48	4.60	3.44	0.41	7.60	1.84
0415	2/2	1.15	3.76	1.85	3.62	7.66	5.42
0206	2/1	4.85	6.04	5.52	0.32	7.94	1.00
1003	7/0	0.38	0.74	0.47	4.20	5.40	4.73

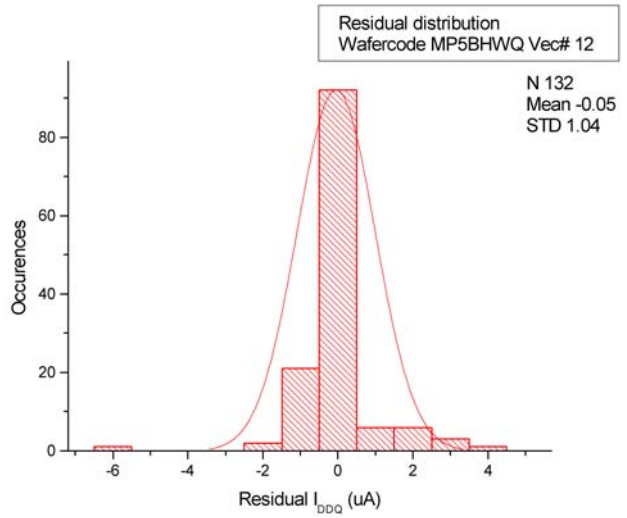

Figure 12: Distribution of residuals

Figure 12 shows the distribution of the residuals for the plane fitting approach. These residuals are plotted against XY coordinates Figure 13. Fault-free chip residual values form a cluster near zero while defective dice have much higher residuals (e.g. a die having residual near 4 μA) and float above the cluster.

Table 2 and 3 summarize a comparison of several limit-setting methods. For the static threshold approach, we used the 5 μA threshold value. For the wafer median approach, the median I_{DDQ} across the wafer for each vector was determined. The threshold value for I_{DDQ} used was computed as:

$$I_{th(i)} = \text{median}_{(i)} + 3\sigma_i$$

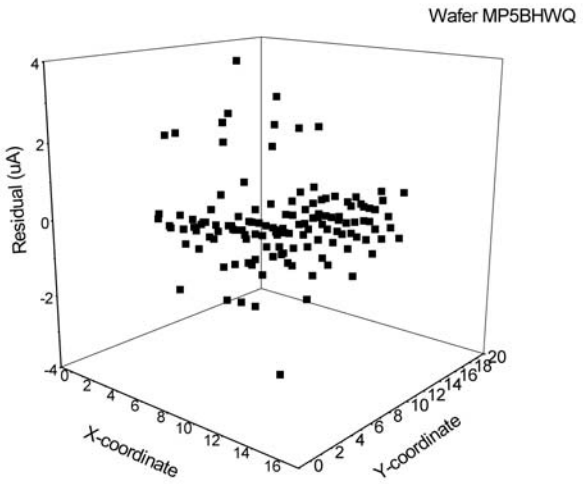

Figure 13: 3-D residual plot

For the delta-I_{DDQ} method, we computed the medians and the standard deviations of the differences between consecutive readings of all dice. If any delta was more than 3σ above the median, the die was rejected. For our implementation of the current signature approach, we followed the same procedure as for delta-I_{DDQ} after sorting all the readings in ascending order. For the plane fit approach, Chauvenet's criterion was first used to reject gross outliers, a plane-fit estimate was computed for I_{DDQ}-only failed dice, residuals were computed for all 195 vectors for all dice on a wafer, and the dice having residuals outside 3σ were rejected. We then used SEMATECH test results to compute the burn-in (BI) fallout, overkill and the defect levels for the different methods. Because we are not certain whether dice with I_{DDQ} above the 5 μA threshold are actually faulty or not, we considered post-BI I_{DDQ}-only failures first as fail and then as pass as shown in Tables 2 and 3 respectively. The actual values will presumably lie in between.

The following formulae were used for computing yield, overkill, and defect level (DL):

$$Yield = \frac{total\ accepted\ chips}{total\ chips} \cdot 100$$

$$Overkill = \frac{rejected\ chips\ passed\ after\ BI}{rejected\ chips\ burned\ in} \cdot (1 - Yield)$$

$$DL = \frac{accepted\ chips\ failed\ after\ BI}{accepted\ chips\ burned\ in} \cdot Yield$$

Table 2: Comparison of different pass/fail limit setting schemes when post-BI I_{DDQ} fails are considered

Test Result	Approach				
	Single Threshold	Wafer Median	Delta I_{DDQ}	Current Signature	Plane Fit
Accept	16644	16001	14464	15993	11099
BI	2215	3652	3143	3075	1419
Fail BI	664	1821	1660	1358	252
% fail	29.97	49.86	52.81	44.16	17.76
Reject	1822	2465	4002	2473	7367
BI	1674	237	746	814	2470
Pass BI	313	33	381	147	697
% pass	18.69	13.92	51.07	18.05	28.22
% Overkill	1.84	1.85	11.06	2.41	11.26
% Yield	90.13	86.65	78.32	86.61	60.11
% DL	27.02	43.21	41.36	38.25	10.67

Table 3: Comparison of different pass/fail limit setting schemes when post-BI I_{DDQ} fails are ignored

Test Result	Approach				
	Single Threshold	Wafer Median	Delta I_{DDQ}	Current Signature	Plane Fit
Accept	16644	16001	14464	15993	11099
BI	2215	3652	3143	3075	1419
Fail BI	539	512	356	297	220
% fail	24.33	14.02	11.32	9.65	15.50
Reject	1822	2465	4002	2473	7367
BI	1674	237	746	814	2470
Pass BI	1555	91	528	454	1392
% pass	92.89	38.39	70.77	55.77	56.36
% Overkill	9.16	5.12	15.33	7.46	22.48
% Yield	90.13	86.65	78.32	86.61	60.11
% DL	21.93	12.14	8.87	8.36	9.32

The yield values are obtained simply by dividing the number of accepted chips by the total number of chips (18466) in the data set. We use the burn-in sample to estimate misclassification of chips. The overkill is the yield loss due to rejecting chips that pass burn-in. This figure includes healing defects. For example, in Table 2, all of the chips that are rejected due to the single threshold test at wafer level would also be expected to fail after burn-in. But as can be seen, 313 pass. In practical production, chips that fail wafer test would be rejected, since too few would heal to justify the packaging and additional testing cost, and healers are a reliability hazard. Thus our overkill figures are higher than if computed using standard practice.

The defect level is assumed to be the burn-in failure rate of accepted chips scaled by the yield. This permits comparison of the absolute number of defective parts for each method. Since the SEMATECH experiment focused on test method evaluation, the sample selected for burn-in was biased towards failed dice, particularly I_{DDQ}-only dice. This explains why defect levels are abnormally high. The high BI fallout rate of accepted chips for the wafer median, delta-I_{DDQ} and current signature test can be explained as follows. Some of the I_{DDQ} readings are several milliamperes, which results in pass/fail thresholds much higher than the other two approaches. This causes many dice with I_{DDQ} above 5 μA to be accepted, which subsequently fail the 5 μA threshold after burn-in. This effect can also explain the difference in accepted and rejected fallout rates between the static threshold and plane fit methods.

Large jumps in deltas between I_{DDQ} values are eliminated in the current signature approach due to sorting, so it accepts more dice than delta-I_{DDQ}. Many of the dice accepted by current signatures have elevated I_{DDQ} for all vectors. Many of these devices fail burn-in, resulting in a lower percentage of accepted chips passing post-BI tests.

It can be seen that each method has its own limitations. The results also underscore how the static-threshold approach is the worst choice for I_{DDQ} testing. When I_{DDQ}-only failures are ignored, it has the highest defect level. Although the yield of the plane-fit method is lower than the other methods, it has by far the lowest defect level in Table 2, and a relatively low one in Table 3, indicating that the dice rejected by this method are indeed defective. However this comes at the cost of the highest overkill. By selecting a less stringent probability threshold and/or residual rejection limit, it is possible to achieve higher yield with a low defect level. As part of a burn-in minimization strategy, thresholds can be set so that accepted dice have sufficiently low defect levels to avoid burn-in, while dice rejected by this method are burned in, rather than being counted as yield loss.

6. Conclusion

This work has demonstrated that the use of spatial information for I_{DDQ} prediction is a valuable technique that allows us to consider process variations while predicting fault-free I_{DDQ} values. It was observed in [25] that the direction of the gradient of the plane is correlated to the speed of the chip. The work here can be extended to use this information by defining I_{DDQ} of a die as a function of the die coordinates and the slope of the plane. Also, the correlation between I_{DDQ} and maximum operating frequency can be exploited for better prediction [29]. Work in this direction will be reported in the future. Also it is possible to correlate the spatial information for reducing early failure rate similar to the work reported in [31]. For the SEMATECH experiment, the burn-in sample was biased towards I_{DDQ}-only failed dice. By using recently obtained post-burn-in data it is possible to resample the dice to minimize the effect of this bias. While it may reduce the sample size considerably, it would be interesting to see what conclusions can be drawn from such an analysis.

Acknowledgements

This research was funded in part by the National Science Foundation under grant CCR-9971102. Thanks to Phil Nigh of IBM for providing the SEMATECH data.

Appendix A: 3-D Least Square Fit

The least squares fit for two dimensions can be found in [26]. We extend this method to three dimensions. The desired plane equation is of the form

$$z(x,y) = A + Bx + Cy$$

where z(x,y) is the I_{DDQ} value for the i^{th} vector for the die whose X and Y coordinates are x and y. We wish to minimize the sum of the squares of errors, that is, perpendicular distances from each $z(x_i,y_i)$ point to the plane. The error function to be minimized is given by

$$E = \sum (z - A - Bx_i - Cy_i)^2$$

Differentiating with respect to A, B and C and equating to zero we obtain:

$$\frac{\partial E}{\partial A} = \sum (z - A - Bx_i - Cy_i) = 0$$

$$\frac{\partial E}{\partial B} = \sum (z - A - Bx_i - Cy_i)x_i = 0$$

$$\frac{\partial E}{\partial C} = \sum (z - A - Bx_i - Cy_i)y_i = 0$$

Rewriting,

$$\sum z_i = AN + B\sum x_i + C\sum y_i$$

$$\sum x_i z_i = A\sum x_i + B\sum x_i^2 + C\sum x_i y_i$$

$$\sum y_i z_i = A\sum y_i + B\sum x_i y_i + C\sum y_i^2$$

where *N* is the total number of points. If data is available for all the neighboring dice and all dice are tested good, *N* would be 8.

For simplicity, we use the following notations:

$$S_x = \sum x_i \ , \ Sy = \sum y_i \ , \ S_z = \sum z_i$$

$$S_{xx} = \sum x_i^2 \ , \ S_{yy} = \sum y_i^2$$

$$S_{xy} = \sum x_i y_i \ , \ S_{xz} = \sum x_i z_i \ , \ S_{yz} = \sum y_i z_i$$

Thus, the above equations can be written as

$$S_z = AN + BS_x + CS_y$$

$$S_{xz} = AS_x + BS_{xx} + CS_{xy}$$

$$S_{yz} = AS_y + BS_{xy} + CS_{yy}$$

Solving simultaneously we obtain,

$$d = NS_{xx}S_{yy} + 2S_xS_yS_{xy} - S_{yy}S_x^2 - S_{xx}S_y^2 - NS_{xy}^2$$

$$A = [S_{xz}(S_{xy}S_y - S_xS_{yy}) + S_{yz}(S_xS_{xy} - S_{xx}S_y) + S_z(S_{xx}S_{yy} - S_{xy}^2)]/d$$

$$B = [S_{xz}(NS_{yy} - S_y^2) + S_{yz}(S_xSy - NS_{xy}) + S_z(S_{xy}Sy - S_xS_{yy})]/d$$

$$C = [S_{xz}(SxS_y - NS_{xy}) + S_{yz}(NSxx - S_x^2) + S_z(S_xSxy - S_{xx}Sy)]/d$$

By substituting values of A, B and C the value of z for a given (x,y) pair can be determined. This is the best fitting plane value.

Appendix B: Rejection of Outliers

Chauvenet's criterion

Chauvenet's criterion is a method to reject outliers in a distribution [27]. It determines the probability that a seemingly illegitimate reading can occur in a data set. If this probability is less than a threshold value, it is discarded. The threshold probability used is usually 0.5.

Assume a data set having *N* readings with the mean and standard deviation μ and σ, respectively. Whether a reading k_{sus} is illegitimate or not is decided as follows:

$$t_{sus} = \frac{k_{sus} - \mu}{\sigma}$$

where t_{sus} is the number of standard deviations by which k_{sus} differs from μ. The probability P(outside t_{sus}·σ) is obtained from the standard probability tables and is multiplied by *N*.

$$n(\text{worse than } t_{sus}) = N \cdot P(\text{outside } t_{sus} \cdot \sigma)$$

If *n* is less than 0.5, the reading is rejected.

Tukey Method

The Tukey method assumes that the distribution is Normal. Two quartile points (*Q1* and *Q3*) are defined such that $1/4^{th}$ of the readings are less than *Q1* and $1/4^{th}$ of the readings are greater than *Q3*. Then the Inter Quartile Range (*IQR*) is defined as

$$IQR = Q3 - Q1$$

The lower quartile limit (*LQL*) and upper quartile limit (*UQL*) are defined as

$$LQL = Q1 - 3IQR$$

$$UQL = Q3 + 3IQR$$

The readings outside of this range are considered outliers. Of course, for I_{DDQ} testing, only the *UQL* is used. Also note that the multiplying factor is a parameter of choice and values other than 3 are often used.

Appendix C: Data transformations

The standard lognormal distribution has a probability distribution function given by [26]

$$f(x) = \frac{e^{-\frac{(\log x)^2}{2\sigma^2}}}{x\sigma\sqrt{2\pi}}$$

The Normal distribution has a probability distribution function given by

$$f(x) = \frac{e^{-\frac{(x-\mu)^2}{2\sigma^2}}}{\sigma\sqrt{2\pi}}$$

To convert a lognormal distribution to the Normal distribution, each I_{DDQ} reading from the set of readings for a vector is divided by the minimum I_{DDQ} for that vector on the wafer (xmin) and the log of the ratio is taken.

$$x(Normal) = \log\left(\frac{x(\log normal)}{x_{\min}}\right)$$

The initial distribution and the distribution for I_{DDQ} readings for a vector on a wafer after transformation are shown in Figures 14 and 15.

We performed a sensitivity analysis of Chauvenet's criterion and results are shown in Figures 16 and 17. These figures show the percentage of the accepted and rejected I_{DDQ}-only chips. A stringent (higher) threshold rejects more potentially-good chips while a lower threshold causes many outliers left in the dataset that can bias the plane estimate higher than the actual. A good threshold value is one that rejects as many outliers as possible without rejecting any of the good chips. Since the distribution of good and bad chips is not known prior to the analysis, a definition of good threshold is debatable. The threshold of 0.5 corresponds to the 3σ limit for the Normal distribution, which is why it is often used. The difference between Figures 16 and 17 highlights the importance of data transformation. Without lognormal transformation, 2 to 6% more chips are rejected.

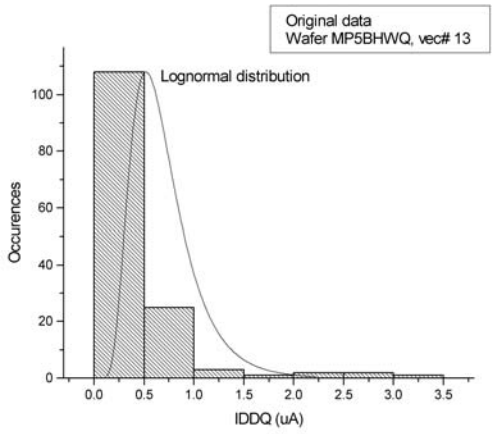

Figure 14 : Lognormal distribution of I_{DDQ} data

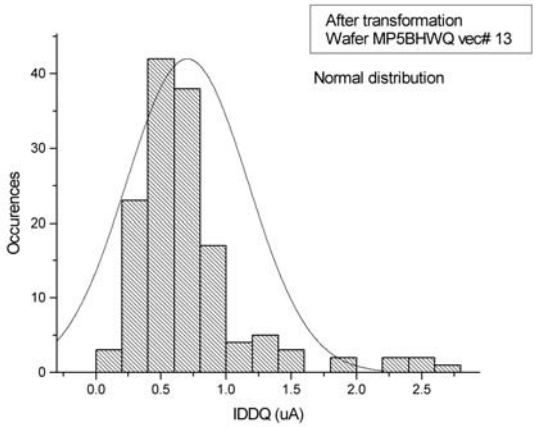

Figure 15: Normal distribution of I_{DDQ} data

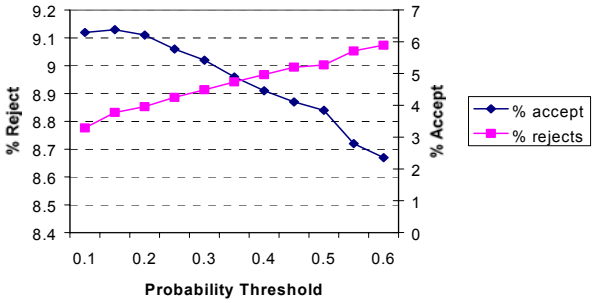

Figure 16: Accept/Reject percentages without lognormal transform

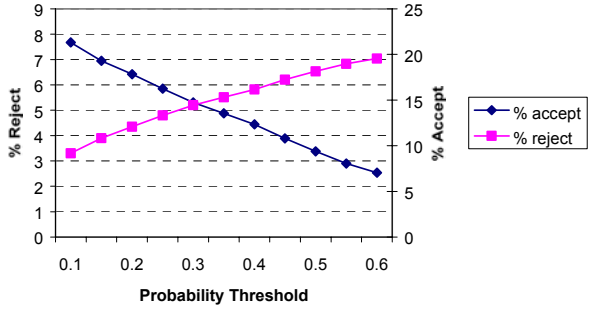

Figure 17: Accept/reject percentages after lognormal transform

References

[1] C. Hawkins et al, "Reliability, Test and I_{DDQ} Measurements", *IEEE Intl. Workshop on I_{DDQ} Testing*, Washington D.C., Nov. 1997, pp. 96-102.

[2] T. Barrette et al., "Evaluation of Early Failure Screening Methods", *IEEE Intl. Workshop on I_{DDQ} Testing,* Los Alamitos, CA, 1996, pp. 14-17.

[3] M. Sachdev, "Deep Sub-micron I_{DDQ} Testing: Issues and Solutions", *European Design and Test Conference,* 1997.

[4] T. Williams et al., "I_{DDQ} Test: Sensitivity Analysis of Scaling", *Intl. Test Conference,* 1996, pp. 786-792.

[5] S. D. McEuen, "I_{DDQ} Benefits", *IEEE VLSI Test Symposium,* 1991, pp. 34-39.

[6] P. Nigh et al., "An Experimental Study Comparing the Relative Effectiveness of Functional, Scan, I_{DDQ} and Delay-Fault Testing", *IEEE VLSI Test Symposium,* 1997, pp. 459-464.

[7] P. Nigh et al., "So what is an Optimal Test Mix? A Discussion of the SEMATECH Methods Experiment," *Intl. Test Conference,* 1997, pp.1037-1038.

[8] D. M. H. Walker, "Requirements for Practical I_{DDQ} Testing of Deep Sub-micron Circuits", *IEEE Intl. Workshop on Defect and Current Based Testing,* Montreal, Canada, May 2000.

[9] T. A. Unni and D. M. H. Walker, "Model-Based I_{DDQ} Pass/Fail Limit Setting", *IEEE Intl. Workshop on I_{DDQ} Testing,* San Jose, CA, Nov. 1998, pp. 43-47.

[10] A. Ferre and J. Figueras, "On Estimating Bounds of Quiescent Current for I_{DDQ} Testing", *IEEE VLSI Test Symposium,* 1996, pp. 106-111.

[11] P. C. Maxwell and J. R. Rearick, "Estimation of Defect-Free I_{DDQ} in Sub-micron Circuits Using Switch Level Simulation", *Intl. Test Conference,* 1998, pp. 882-889.

[12] T. Henry and T. Soo, "Burn-in Elimination of a High Volume Microprocessor using I_{DDQ}", *Intl. Test Conference,* 1996, pp. 242-249.

[13] A. Gattiker and W. Maly, "Current Signatures", *VLSI Test Symposium,* Princeton, New Jersey, April 1996, pp. 112-117.

[14] B. Laquai et al., "A Production-Oriented Measurement Method for Fast and Exhaustive I_{DDQ} Tests", *European Design and Test Conference,* 1997.

[15] C. Thibeault, "On the Comparison of I_{DDQ} and ΔI_{DDQ} Testing", *IEEE VLSI Test Symposium,* 1999, pp.143-150.

[16] C. Thibeault, "Improving Delta- I_{DDQ} -based Test Methods", *Intl. Test Conference,* 2000, pp. 207-216.

[17] A. Miller, "I_{DDQ} Testing in Deep Sub-micron Integrated Circuits", *Intl. Test Conference,* 1999, pp. 724-729.

[18] P. Maxwell et al., "Current Ratios: A Self-scaling Technique for Production I_{DDQ} Testing", *Intl. Test Conference,* 1999, pp. 738-746.

[19] S. Jandhyala et al., "Clustering Based Techniques for I_{DDQ} Testing", *Intl. Test Conference,* 1999, pp. 730-737.

[20] A. D. Singh, "A Comprehensive Wafer Oriented Test Evaluation (WOTE) Scheme for the I_{DDQ} Testing of Deep Sub-Micron Technologies", *IEEE Intl. Workshop on I_{DDQ} Testing,* 1997, pp. 36-39.

[21] A. D. Singh et al., "Screening for Known Good Die Based on Defect Clustering: An Experimental Study", *Intl. Test Conference,* 1997.

[22] A. D. Singh et al., "Binning for IC Quality: Experimental Studies on the SEMATECH Data", *Intl. Symposium on Defect and Fault Tolerance in VLSI Systems,* 1998.

[23] W. R. Daasch et al. "Variance Reduction Using Wafer Patterns in I_{DDQ} Data", *Intl. Test Conference,* Atlantic City, Oct. 2000, pp. 189-198.

[24] V. Ramakrishnan and D. M. H. Walker, "IC Performance Prediction System," *Intl. Test Conference*, 1995, pp. 336-334.

[25] J. Lee and D. M. H. Walker, "IC Performance Prediction for Test Cost Reduction," *Intl. Symposium on Semiconductor Manufacturing*, *Santa Clara, CA*, Nov. 1999.

[26] J. Miller, "Statistics for Advanced Level," *Cambridge University Press*, 1994, pp. 345-367.

[27] J. R. Taylor, "An Introduction to Error Analysis," *University Science Books*, 1982, pp. 141-146

[28] R. Richmond, "Successful Implementation of Structured Testing," *Intl. Test Conference*, 2000, pp. 344-348.

[29] A. Keshavarzi et al., "Intrinsic Leakage in Deep Submicron CMOS IC – Measurement-Based Test Solutions", *IEEE Trans. on VLSI Systems,* Dec. 2000, pp. 717-723.

[30] S. Meyer, "Data Analysis for Scientists and Engineers," *John Wiley & Sons*, 1975, pp.17-18.

[31] K. Wallquist, "On the Effect of I_{SSQ} Testing in Reducing Early Failure Rate," *Intl. Test Conference*, 1995, pp. 910-915.