Immediate Neighbor Difference I_{DDQ} Test (INDIT) for Outlier Identification

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Abstract

Increasing values and spread in leakage current makes it impossible to distinguish between faulty and fault-free chips using single threshold method. Neighboring chips on a wafer have similar fault-free properties. By obtaining differences in I_{DDQ} values it is possible to discriminate faulty dice. In this paper, a technique in which comparison of I_{DDQ} of a die with that of its neighboring dice on the wafer is evaluated. The analysis based on the SEMATECH test data[§] is presented.

Keywords: I_{DDQ} testing, delta I_{DDQ}, spatial correlation

1. Introduction

With reducing transistor geometries and the corresponding reduction in threshold voltages, leakage currents increase exponentially [1]. This makes it difficult, if not impossible, to distinguish between faulty and fault-free leakage current (I_{DDQ}) values. Traditional single pass/fail threshold scheme causes unacceptable yield loss and/or test escapes [2]. This is worsened due to increased process variations. Several schemes have been reported in the literature to resolve this problem [3].

Fundamentally there are different ways to approach the problem: either to reduce the background leakage or to estimate the fault-free I_{DDQ} as accurately as possible or to use data analysis methods to discriminate faulty I_{DDQ} from fault-free I_{DDQ}. Fault-free I_{DDQ} can be estimated by developing more accurate transistor or cell models [4],[5]. However, this is difficult due to increased process variations. Alternatively, faulty I_{DDQ} can be distinguished by different methods like current signature [6], delta I_{DDQ} [7],[8], clustering [9], or current ratios [10]. All these methods rely on some sort of statistical or graphical analysis of I_{DDQ} data. Use of I_{DDQ} of neighboring dice on a wafer for estimating fault-free I_{DDQ} of the center die has been investigated [11]. In this paper we evaluate the combination of the conventional delta-I_{DDQ} technique and wafer-level neighboring die information. The difference between neighboring dice and the center die's I_{DDQ} is used to determine whether the center die is fault-free or not. The analysis of the SEMATECH data is presented. The goal of this paper is *not* to find a better threshold setting method but to detect chips that show markedly different properties than their neighbors and, therefore, are deemed defective. The remainder of the paper is organized as follows. In the next section we discuss the motivation behind this concept. Section 3 outlines the analysis procedure. Section 4 discusses the experimental results and finally Section 5 concludes the paper.

[§] This data comes from the Test thrust at SEMATECH, Project S-121 on Test Methods Evaluation. The conclusions drawn are our own and do not necessarily represent views of SEMATECH or its member companies.

2. Motivation

As transistor geometries are reduced, for constant field scaling supply voltage is reduced. To obtain high performance under reduced supply voltage it is necessary to reduce the threshold voltage. This results in an exponential increase in the leakage current [3].

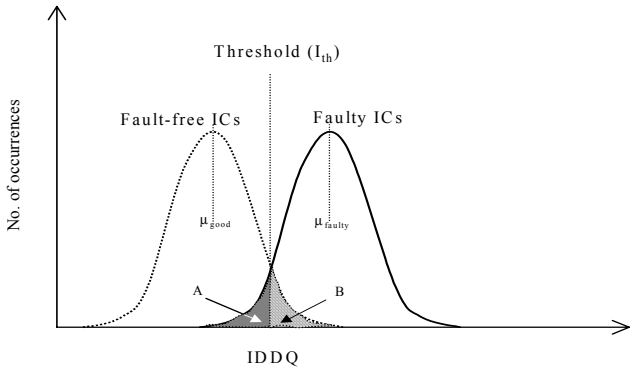

Figure 1: Fault-free and faulty I_{DDQ} distributions overlap for DSM technologies

In earlier technologies, I_{DDQ} testing was achieved by selecting a single threshold value. If the leakage current of a chip exceeded the threshold for any vector, the chip was considered defective. The detection of defective chips in this way is possible only if one of the vectors excites the defect and the faulty I_{DDQ} is much higher than the fault-free I_{DDQ}. However, increased leakage in deep sub-micron (DSM) technologies causes fault-free and faulty I_{DDQ}

distributions to overlap as shown in Figure 1. Hence it is impossible to distinguish between faulty and fault-free chips using single threshold method. Such a method inevitably results in the yield loss (region B in Figure 1) and/or the test escapes (region A in Figure 1). The overlap between these two distributions would increase as transistor geometries are scaled further [2]. Thus distinguishing faulty I_{DDQ} from the fault-free (background) leakage is increasingly difficult. In fact, the International Technology Roadmap for Semiconductors (ITRS) considers this to be a difficult challenge for future technologies [12].

Due to similar manufacturing conditions, fault-free device parameters of neighboring chips on a wafer are highly correlated. Thus neighboring chips on a wafer have similar fault-free I_{DDQ} for the same vector. Figure 2 shows the wafer level variation in I_{DDQ} for a vector. The dice that failed the Boolean tests (functional, stuck-at or AC scan delay tests) are indicated by blank spaces. Notice that there is very small variation in the "fault-free" leakage current across the wafer. Some of the defective chips have I_{DDQ} more than an order of magnitude greater than that of the neighboring dice and hence appear as *spatial outliers*. Since there is no physical mechanism that can explain why these dice have such high current and still be fault-free, they definitely pose considerable reliability risk (even if they pass all Boolean tests). Thus by comparing I_{DDQ} of the center die to its neighboring die I_{DDQ} it should be possible to determine whether center die is fault-free or not. This is the basic theme explored in this work.

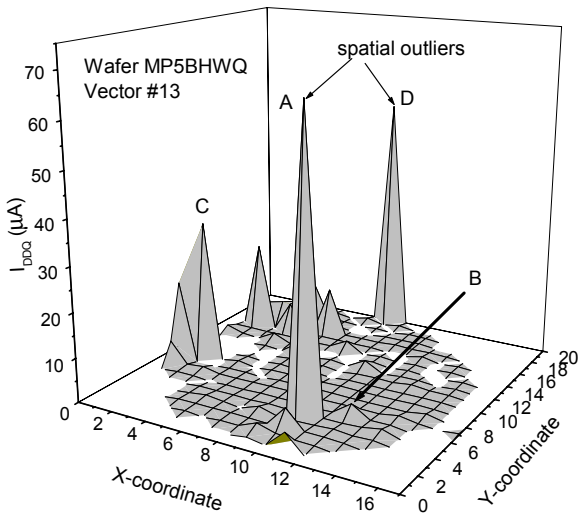

Figure 2: Neighboring fault-free chips have small I_{DDQ} variation, defective chips appear as "spatial outliers"

The concept of delta I_{DDQ} has been proposed earlier [7], [13]. In the conventional delta I_{DDQ} method, differences (deltas) between I_{DDQ} values for different vectors for a chip are obtained. For a fault-free chip, only intrinsic variation in I_{DDQ} causes the mean delta I_{DDQ} to be close to or equal to zero and the variation in deltas to be small. This method assumes that at least one vector excites the defect and the defective I_{DDQ} is much higher than the fault-free I_{DDQ}. In case of a passive defect since all readings are elevated, deltas are small. Hence this method is unable to screen chips with a passive defect. Figure 3 illustrates the histograms of delta I_{DDQ} for three neighboring dice from a wafer. All these dice passed the Boolean tests. In each case, a total of 194 deltas are obtained by subtracting readings for the two consecutive vectors. Figure 3(a) is a fault-free die (0518) that exhibits small mean value and variation. Figure 3(b) illustrates the histogram for a die (0619) with an active defect. Such a die typically exhibits large variation in delta I_{DDQ}. Figure 3(c) underscores the difficulty in screening a die with passive defect (0519) as the variation in deltas in not considerably large. However, notice that this die could have been detected to be defective by comparing its I_{DDQ} values to its fault-free neighboring die (0518). This is main idea behind INDIT as explained in the next section.

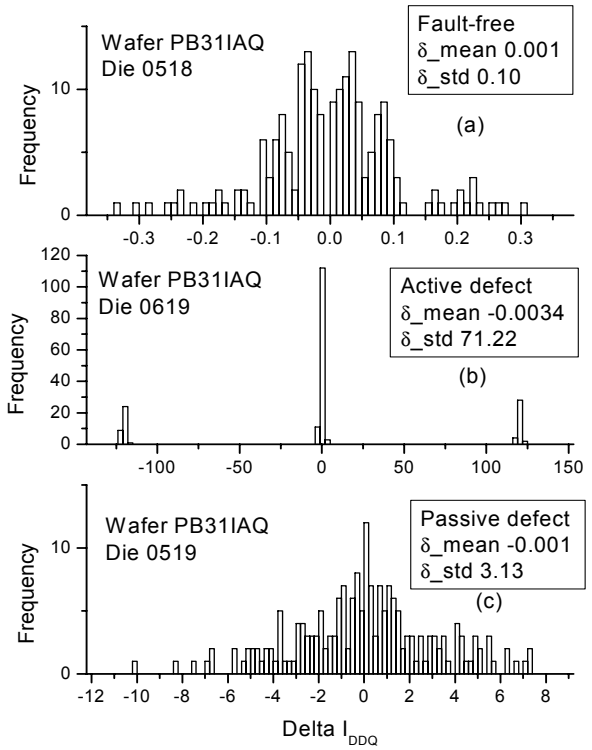

Figure 3: Delta I_{DDQ} histogram for a fault-free die(a), for a die with active defect (b) and for a die with passive defect (c)

3. INDIT Algorithm

Immediate **N**eighbor **D**ifference $\mathbf{I}_{DDQ}$ **T**est (INDIT) relies on the observation that neighboring chips on a wafer have similar fault-free I_{DDQ} values for the same input vector. Thus difference between these values should be very small. If the center die has leakage current much higher than any of its neighbors, it is likely to contain a defect. Conversely, if the center die has smaller leakage

N1	N2	N3
N4		N5
N6	N7	N8

Figure 4: Immediate neighboring dice for INDIT

current than all its neighbors, the neighboring dice are likely to be defective.

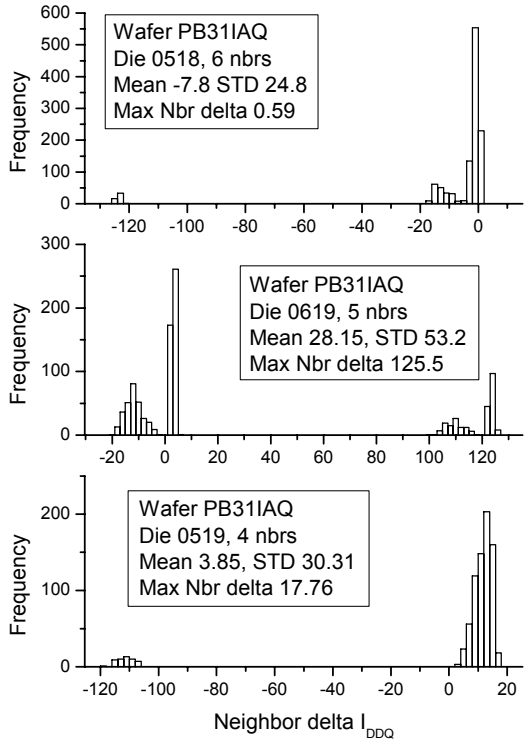

Figure 5: Neighbor-delta I_{DDQ} for three dice shown in Fig. 3

Screen all dice that fail Boolean test
For each remaining dice on a wafer
Find number of immediate neighbors (I_n) available
If (I_n>0){
For each neighbor $N_i \in \{N1..N8\}$
For each vector j
Nbr Delta(j) = Center die $I_{DDQ}(j)$- N_i I_{DDQ} (j)
Find maximum neighbor-delta for N_i
Find maximum neighbor-delta δ_{max}
}
If δ_{max} > threshold reject the die

Figure 6: INDIT algorithm

For a die on a wafer we consider eight immediate neighboring dice (marked N1 through N8) as shown in Figure 4. Dice on the wafer edge have fewer immediate neighbors. A die with no immediate neighbors is ignored from the analysis. Also neighboring chips that fail any Boolean test are ignored. This can result in having less than eight neighbors for a non-edge die. For each vector the difference between I_{DDQ} readings is obtained by subtracting neighboring die I_{DDQ} value from that of the center die. To distinguish a delta between different vectors for the same chip from a delta between different chips for the same vector, we denote the former by *self-delta* and the later by *neighbor-delta*. The maximum neighbor-delta for each vector is used for pass/fail decision. The I_{DDQ} values for the same vector for two fault-free dice are expected to be similar. Thus fault-free dice would yield small neighbor-deltas owing to local intrinsic process variation. In a fault-free wafer zone, process variations would cause neighbor-deltas to be positive as well as negative and the mean value would be close to zero.

Figure 5 shows neighbor-deltas for the three dice shown in Figure 3. In each case a total of 195 deltas for each neighbor are obtained. The fault-free die (0518) has negative mean indicating its neighboring dice have much higher leakage. (at least one neighbor has leakage current two orders of magnitude more than the center die). The die with active defect (0619) shows much higher positive mean and large standard deviation in neighbor-deltas and can be easily identified by observing three clusters in the histogram. The cluster near –10 (100) occurs due to vectors that excite defect(s) in the neighboring dice (center die) but not the center die (neighboring dice). The third cluster near 0 occurs when neither defect is excited. In fact, this histogram shows that there is at least one more die in the neighborhood that has a pattern-dependent (active) defect. The die with passive defect (0519) shows two clusters. The clear positive shift in the distribution and the mean value indicates the presence of passive defect. Thus the neighboring dice can provide valuable information indicating whether the center die is fault-free or not and, if it is faulty, about the nature of defect (active/passive and severity of the defect). The INDIT algorithm is outlined in Figure 6.

Figure 7 shows the wafer plot for maximum self-deltas for the same wafer shown in Figure 2. The dice identified as "A", "B" and "C" are clearly spatial outliers. I_{DDQ} value for "B" was low for the vector selected in Figure 2. However, some vectors excited the defect resulting in peaks in Figure 7. On the other hand, the die "D" (in Figure 7) that appears as an outlier in Figure 2, does not show large self-deltas. This is indicative of a passive defect. The maximum neighbor-deltas for dice on this wafer are plotted in Figure 7. The chips A, B and C clearly appear as outliers. Notice that D now clearly appears as an outlier. Moreover, many dice (marked E through H) that are not detected by self-delta can now be identified as outliers. Die F does appear as an outlier in Figure 7. However, INDIT improves the confidence in outlier detection (see Figure 8).

Different cases for INDIT are discussed as follows:

(a) A die with active defect in good neighborhood

If the center die has an active defect and all the neighboring dice are fault-free, the neighbor-deltas are large positive values for vectors that excite the defect. This results in high positive neighbor-delta.

(b) A die with passive defect in good neighborhood

For a die with passive defect in the fault-free neighborhood, all neighbor-deltas are positive. This would result in high mean value of neighbor delta.

(c) A good die in a defective cluster

If all the neighboring dice for a fault-free die are defective (passive/active), the maximum neighbor-delta in the worst case is a small positive number. Such dice are more likely to contain subtle defects due to defect clustering and pose reliability concern [14].

(d) A defective die in a defective cluster

For a defective die surrounded by defective dice, neighbor-deltas depend on the nature of defect and are rather unpredictable. The probability that both chips have identical defective currents is negligible for practical purposes. The neighbor-delta value depends on the relative severities of defects.

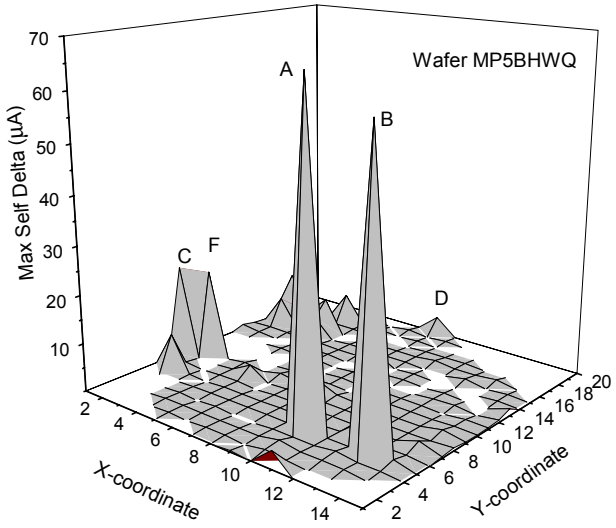

Figure 7: Wafer surface plot of maximum self-deltas

4. Experimental Results

We used SEMATECH data for evaluating INDIT. In the SEMATECH experiment four types of tests were conducted on 18466 chips at the wafer level. These include functional, stuck-at scan, AC scan delay test and I_{DDQ} test. A total of 195 measurements were taken for I_{DDQ} test. If any measurement exceeded the pass/fail limit of 5 µA the chip was considered I_{DDQ} fail. This limit was selected based on the distribution of the entire population and did not specify good manufacturing limit [15]. A sample of chips was packaged and subjected to six hours of burn-in (BI) and all tests were conducted again. We limited our analysis to the BI sample. We screened chips that fail functional, stuck-at or delay tests at the wafer level. We also screened chips that had I_{DDQ} more than 100 µA for any vector. Chips having leakage current above 100 µA were assumed to contain gross defect [16]. These chips appear in the tail of the distribution and are screened due to reliability concerns.

The total number of chips in the data set is 1941. The distribution of these wafer level and post-BI results of these chips is shown in Table 1. A total of 225 wafer-level I_{DDQ}-only failed chips pass I_{DDQ} test after burn-in exhibiting healing defect. These chips are essentially unreliable and are rejected in the test flow.

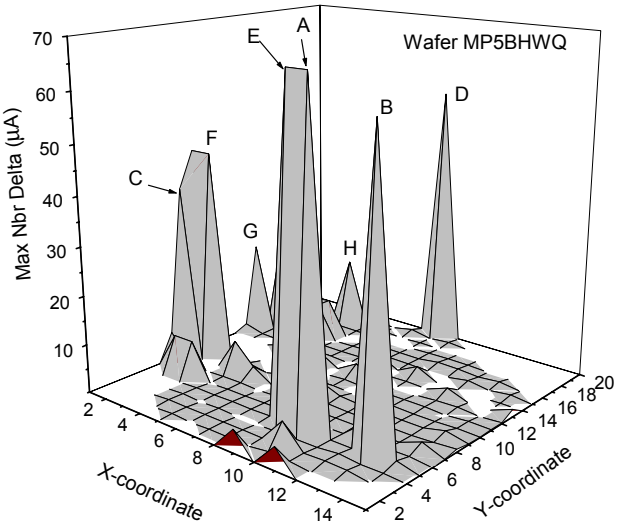

Figure 8: Wafer surface plot with maximum neighbor-deltas

Table 1: Distribution of wafer test and post BI results of chips in the dataset

Wafer Test Result	Post Burn-in result		
	All pass	I_{DDQ}-only fail	Other fail
All pass	1052	27	19
I_{DDQ} fail	225	598	20

Deciding Pass/Fail Criterion

The comparison with neighboring chips makes identification of outlier (defective) chips easier. However, this does not come as a panacea to pass/fail limit setting. The appropriate threshold for neighbor-delta for rejecting defective devices must be determined.

Figure 9 shows the cumulative distribution of maximum self-deltas and maximum neighbor-deltas. A total of 8 chips that passed all tests and had negative maximum neighbor-deltas (good chips in bad neighborhood) are not included while plotting the neighbor-delta CDF. Figure 9 shows that 90% of maximum self-deltas are less than 16 µA. We therefore selected a self-delta pass/fail threshold of 16. Figure 10 highlights the distinction between CDFs for self

and neighbor-deltas for chips that pass all tests and fail I_{DDQ}-only test at wafer. Chips that pass all tests have noticeable sharp rise in both the CDFs since they have similar I_{DDQ} values. Although by definition, I_{DDQ}-only failed chips have at least one reading greater than 5 µA, notice that a ~5 % I_{DDQ}-only failed chips have maximum self-deltas less than 1 µA and neighbor-deltas less than 5 µA.

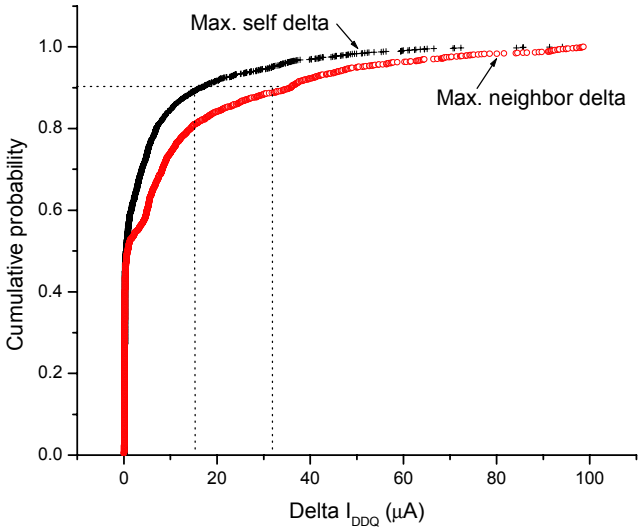

Figure 9: CDFs for maximum self and neighbor-deltas

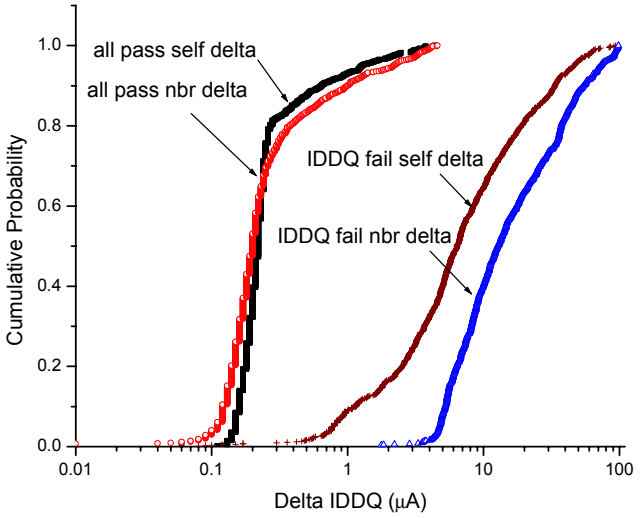

Figure 10: CDFs for self and neighbor-deltas of chips with different wafer probe results

The defect level (DL) and overkill were computed by observing post-burn-in results. The DL was computed using the following formula:

$$DL = \frac{Number\ of\ accepted\ chips\ that\ fail\ boolean\ tests\ after\ BI}{Total\ number\ of\ chips\ accepted}$$

The overkill was computed using the following formula:

$$Overkill = \frac{Number\ of\ rejected\ chips\ that\ pass\ all\ tests\ after\ BI}{Total\ number\ of\ chips\ rejected}$$

The healers are not counted while computing overkill.

To compare the effectiveness of INDIT procedure in screening defective chips not detected by self-delta, the neighbor-delta threshold was varied so as to achieve nearly the same DL as self-delta. (Due to discontinuous uneven distribution of neighbor-deltas, it is difficult to match DLs exactly). The neighbor threshold of 60 gave the closest obtainable DL. Table 2 shows the distribution of the chips in two methods.

Table 3 shows DL and overkill values for these two methods. Since both thresholds are quite loose, none of the chips from "All pass" category get rejected by any method. The distinction appears for I_{DDQ}-only failed chips. We ignore healers from the analysis due to their reliability concerns. Both methods reject a majority of I_{DDQ}-only failed chips.

Table 2: Distribution of chips according to SEMATECH test results for self-delta and neighbor-delta test methods

Wafer Probe Result	Self-delta accept		Self-delta reject		Post BI result
	N-delta accept	N-delta reject	N-delta accept	N-delta reject	
All pass	1052	0	0	0	All Pass
	27	0	0	0	I_{DDQ} Fail
	19	0	0	0	Other Fail
I_{DDQ} fail	206	1	13	5	All Pass
	394	24	138	42	I_{DDQ} Fail
	17	1	2	0	Other Fail

Table 3: DL and Overkill comparison of two methods

Method	DL (%)	Overkill (%)	Apparent Yield %
Self-delta	2.13	99	89.7
Nbr-Delta	2.03	98.6	96.2

Figure 11 shows the distribution of post-BI results of chips for different maximum neighbor-delta values. A high percentage of chips having small neighbor-deltas (< 2 µA) pass all post-BI tests. The healers do not exhibit any specific trend. A majority of chips having large neighbor-deltas (> 10 µA) fail I_{DDQ} test or Boolean tests after BI.

5. Conclusions and Future Work

Comparing intra-die variation in I_{DDQ} with that of the neighboring dice on the wafer is helpful in detecting spatial outlier chips that are likely to fail during/after burn-in (infant mortality). A methodology that uses wafer-level spatial information is proposed in this paper. Experimental results show that for the same DL targets, higher yields and comparable or lower overkill can be achieved.

INDIT can be easily integrated in the conventional test flow. The wafer level post-processing can be done during the shadow time while another wafer is being loaded thus with little impact on the test time. Outlier identification thresholds must be empirically determined so as to achieve lower DL targets without compromising on overkill or having excessive yield loss. Spatial outliers detected by INDIT can be selectively burned in or simply rejected earlier in the test flow. This can result in dramatic test cost reduction.

Some wafers exhibit stepper field, which can lead to higher overkill when INDIT is used. By correlating another test parameter like delay it might be possible to separate "benign" spatial outliers that do not lead to infant mortality.

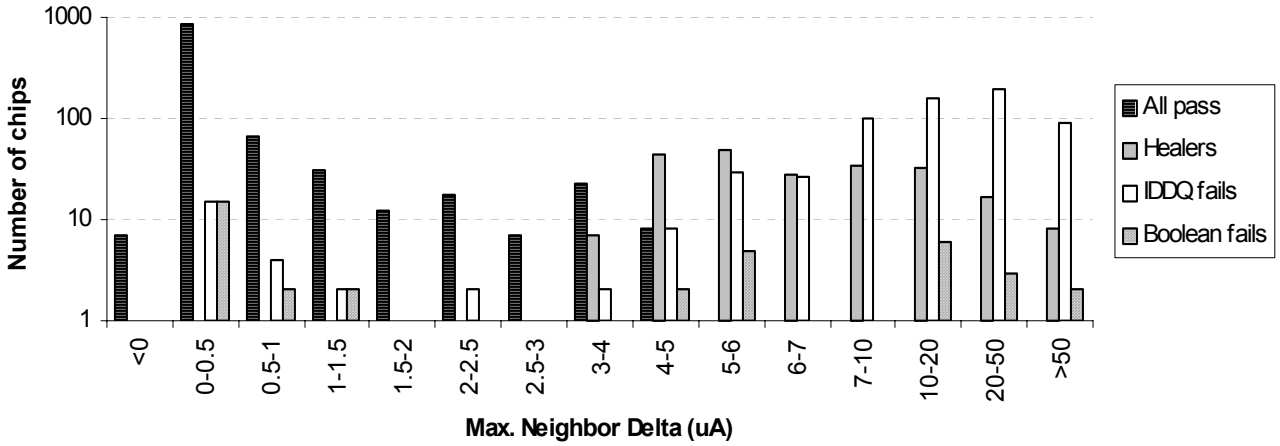

Figure 11: Distribution of post-BI results of chips for different maximum neighbor-delta values

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